From Device Engineer to device Astrologer!!!

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My agenda

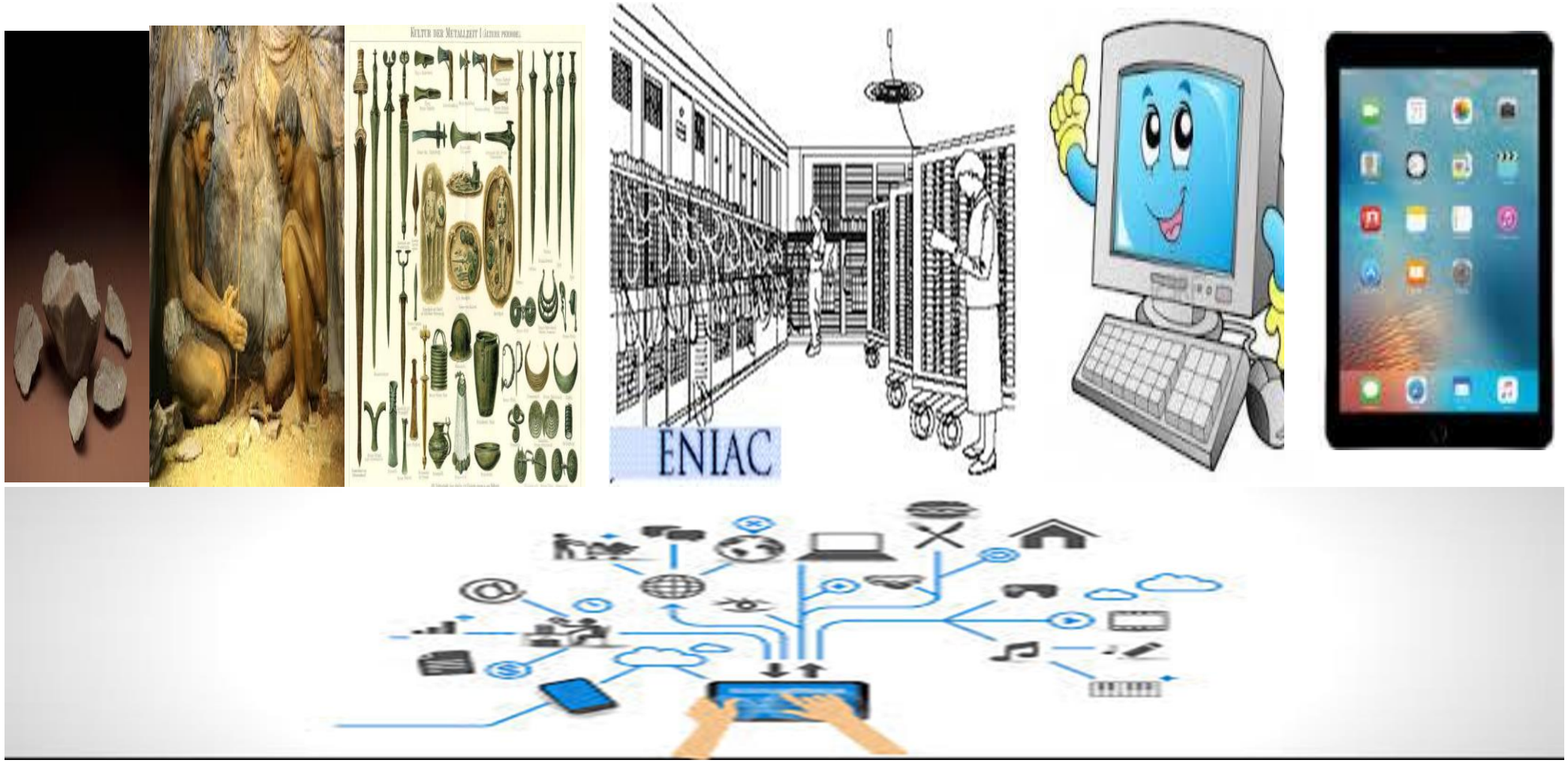
1.History/evolution(how we have reached here!!)

2.Problem Of Plenty!!/Challenges and opportunities

3.Device astrology!!What/Why/how etc

4.Hands on!!

Evolution in human technology



We now want to replace us also

- Giving intelligence to the systems we have created so that it can take its own decisions/smart systems and now IoT or IoE(Internet of everything)

Role of electronics engineer? Scientists vs engineers

- Scientists come out with laws governing the nature of things
- Engineers put those laws in action/(use them to develop useful gadgets which enable us to do many things which could not have been done otherwise)
- Engineering a single product involves use of multiple laws and same law may be used to engineer multiple products

Task in hand of an electronics engineer

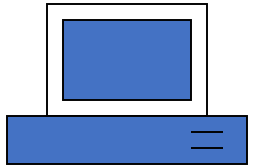
- Electronic gadgets-Do I have to name them??
- Gadget/system what is it? It offers you function(s) take the example of a state of the art cell phone?
- Now how this functions are obtained? Circuits
- What is a circuit?
- “A sentence is a group of words which *make some sense”*
- That brings us to devices

Parts of an electronic system!

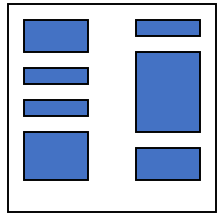
Hierarchy

Various levels of hierarchy

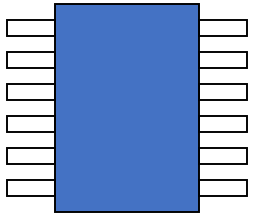
System



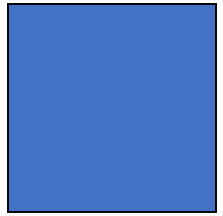
Board

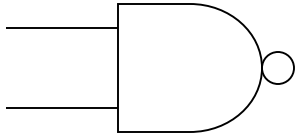


Chip

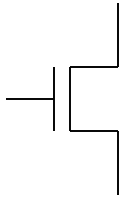


Block

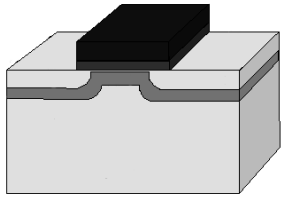




Logic



Transistor

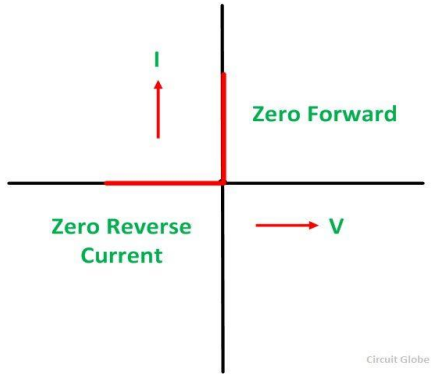


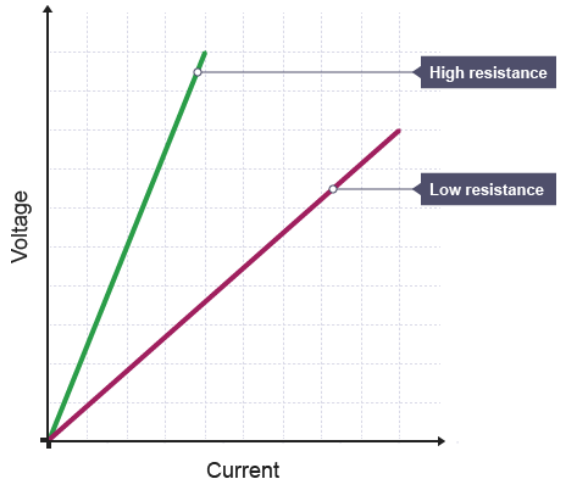
Device

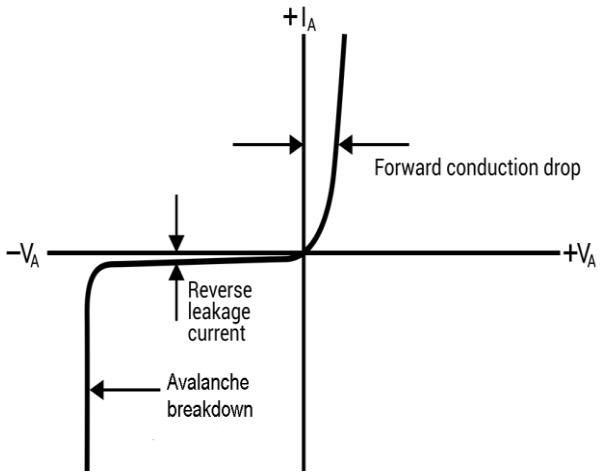
Device abstractions

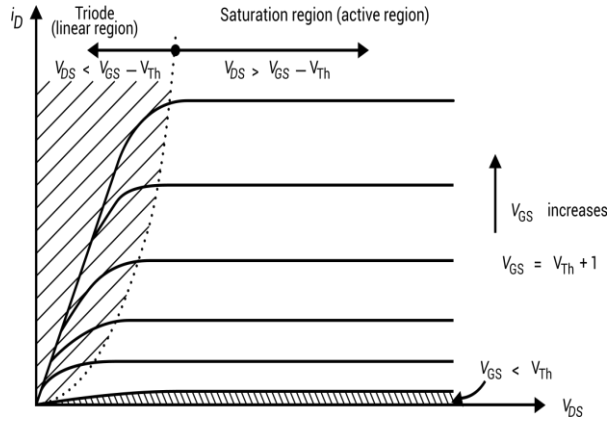
- Functionality is obtained by circuits-circuits are obtained by combination of devices.
- Devices are selected by their character(istics)- mainly I-V characteristics- what is the nature of current flow for the given applied voltage.
- Good to look for abstractions in device characteristics

Abstractions in device characteristics









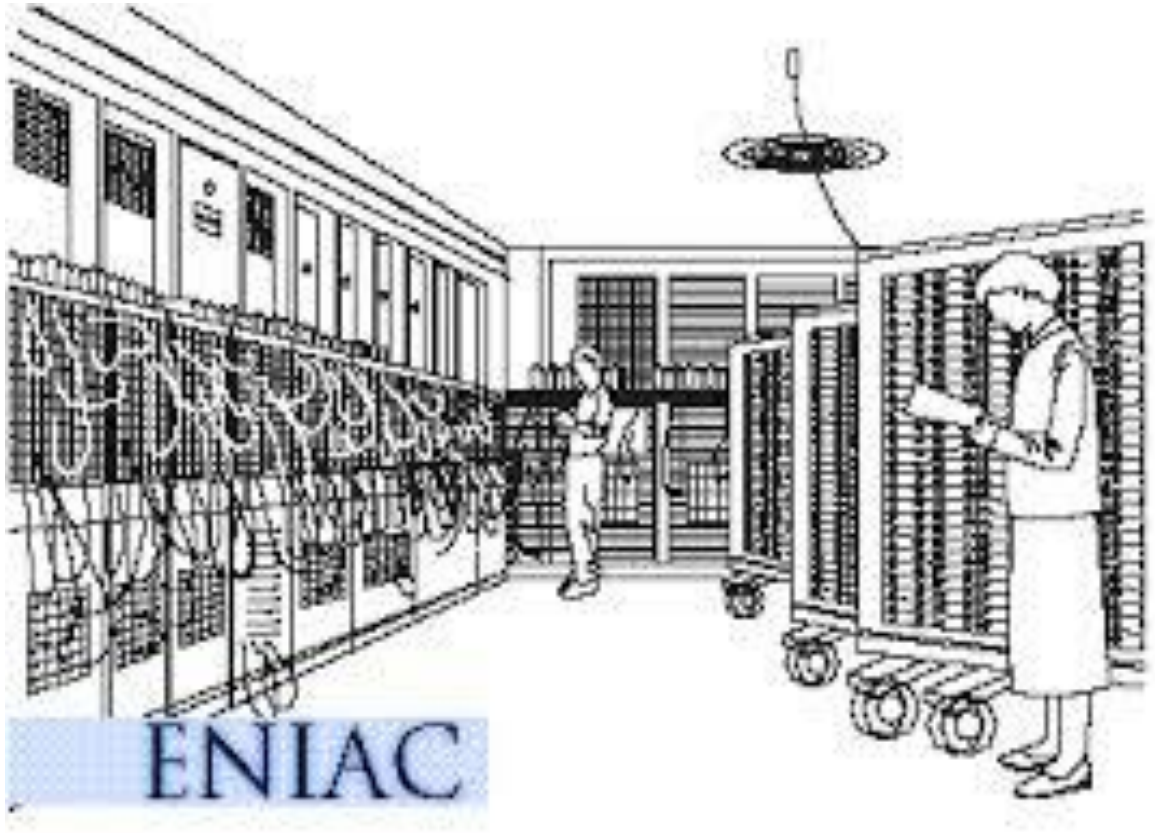
The roads we have travelled-Vacuum tube era

- Electronics started with this
- Our electronics systems were based around them
- Radio, TV etc

We have built this also with it!!

Electronic Numerical Integrator and Computer

in 1956, ENIAC contained 20,000 vacuum tubes, 7200 diodes, 1500 relays, 70,000 resistors, 10,000 capacitors and approximately 5,000,000 hand-soldered joints. It weighed more than 27 tons), was roughly 2.4 m × 0.9 m × 30 m (8 × 3 × 100 feet) in size, occupied 167 m^2 (1,800 ft^2) and consumed 150 kW of power. Several tubes burned out almost every day, leaving ENIAC non-functional about half the time. (Ref: Wikipedia)



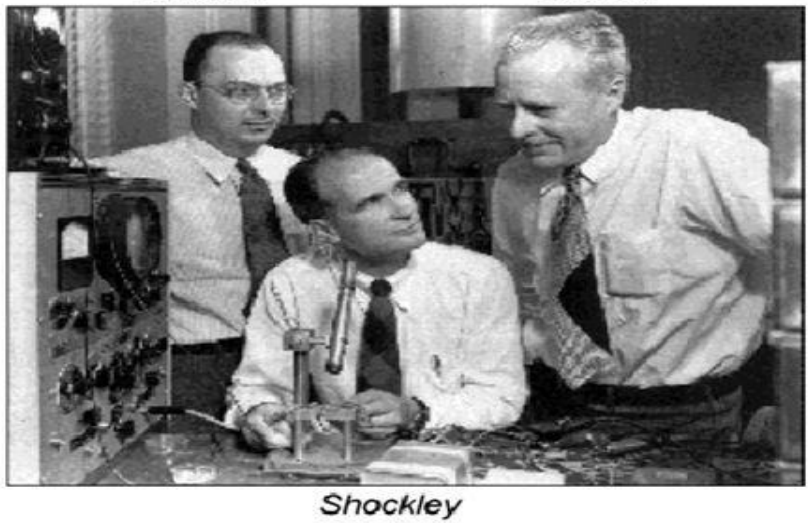
Solid state device era

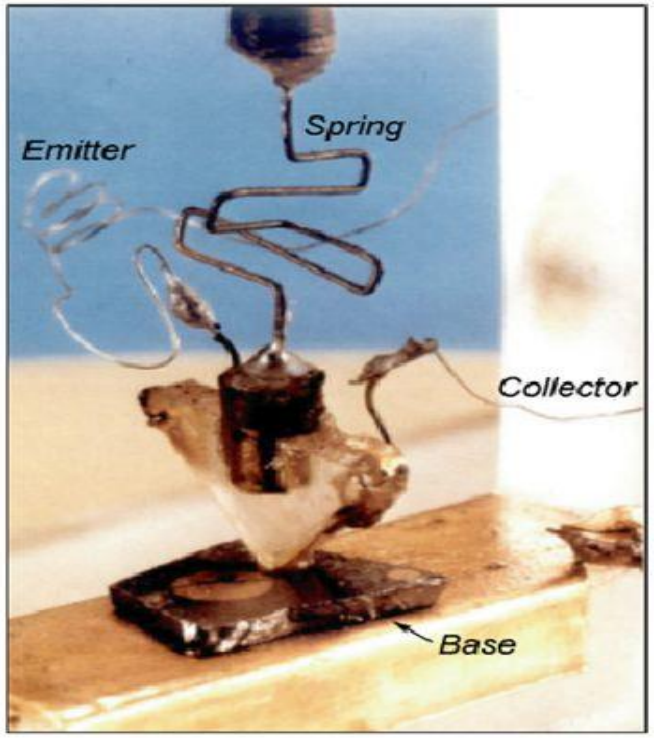
Point-Contact Transistor – first transistor ever made

The first transistor was a point-contact transistor

The first point-contact transistor

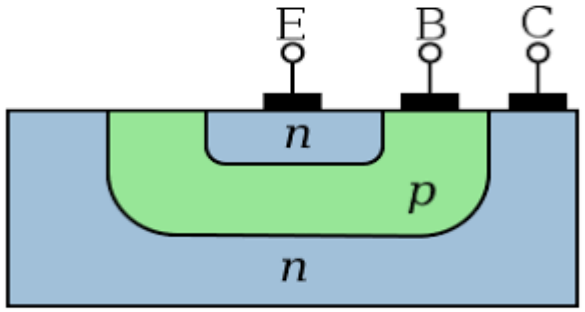
John Bardeen, Walter Brattain, and William Shockley
Bell Laboratories, Murray Hill, New Jersey (1947)

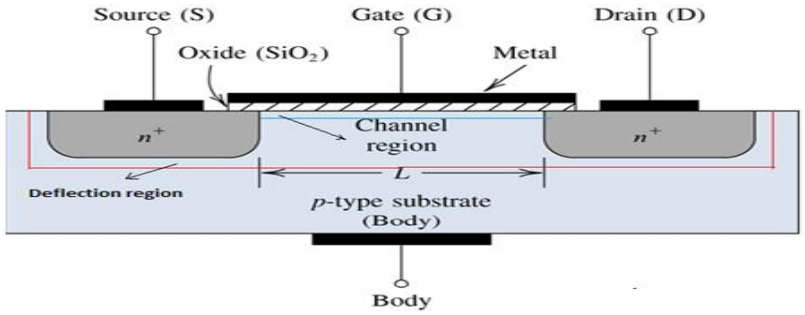




Categories of semiconductor devices based on conduction mechanism

- Diffusion based-PN junction based examples: diode, BJT etc
- Field effect devices-based on drift current-MOSFET's

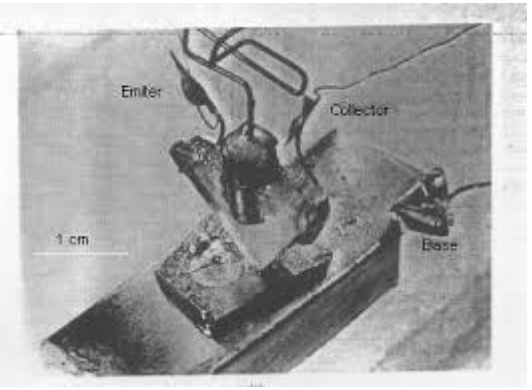




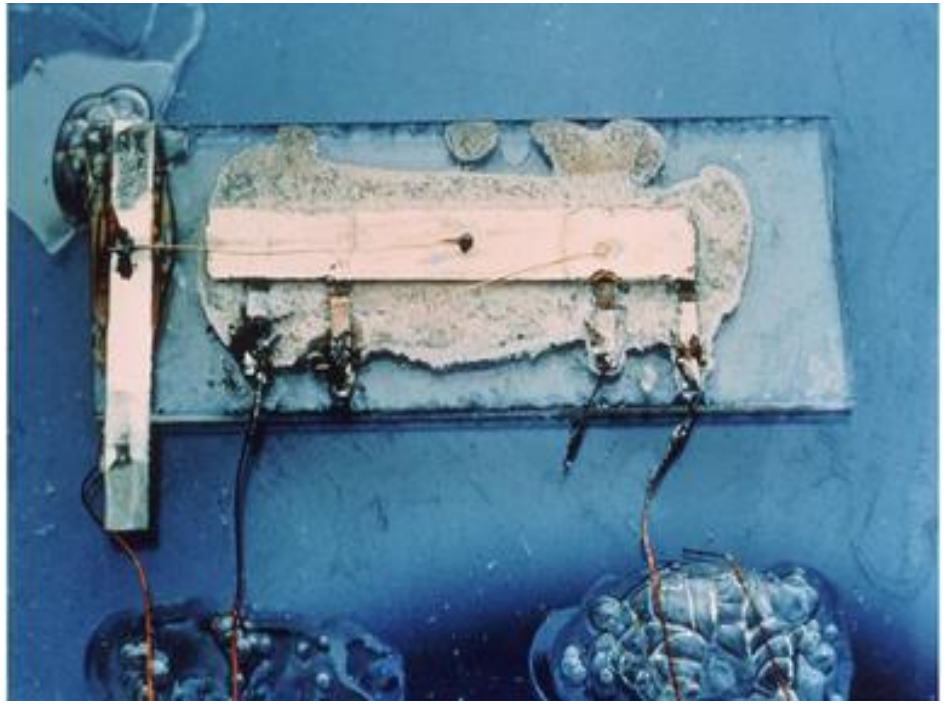
Solid state based electronic systems

PN junction era-Bipolar era

- 1947 to 1964



Beginning of integrated circuits(1958-



First Silicon IC Chip Made by Robert Noyce of Fairchild Camera in 1961

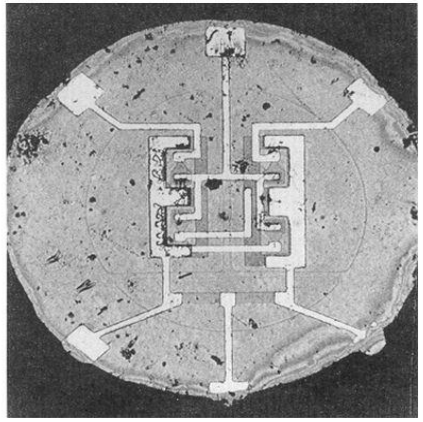
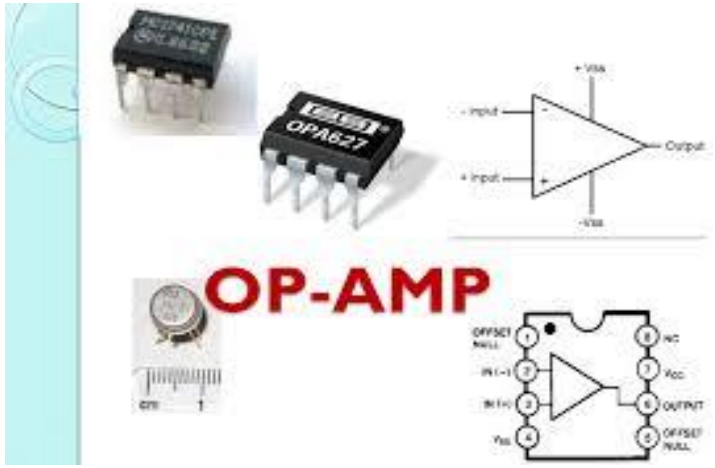
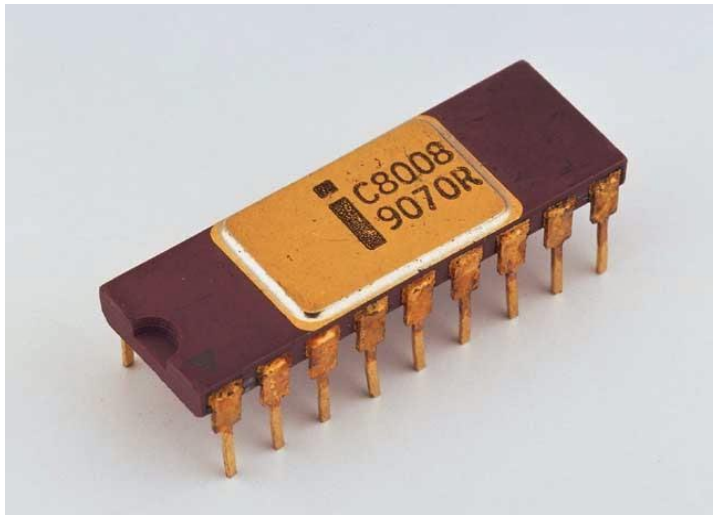


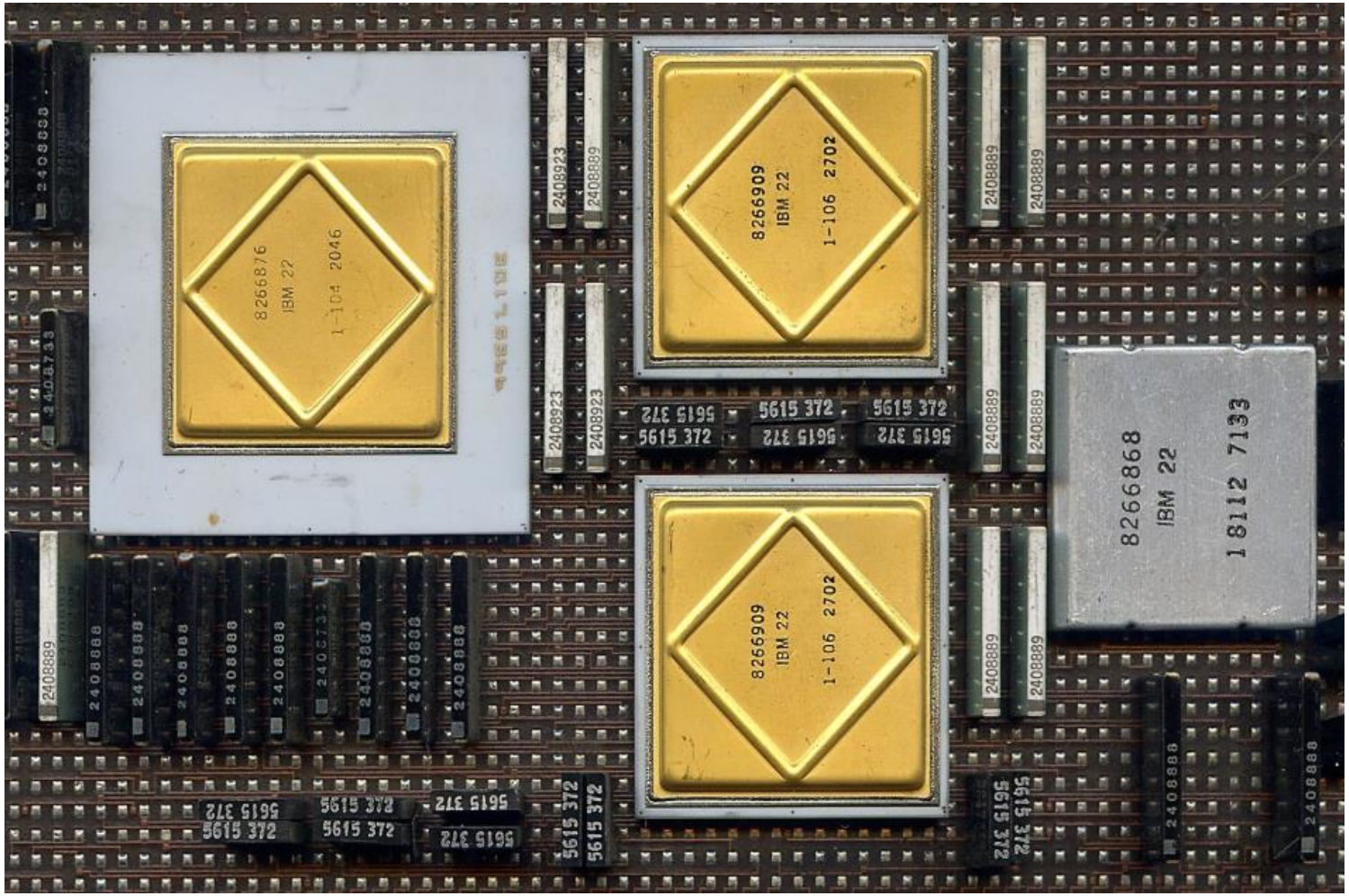
Photo courtesy: Fairchild Semiconductor International

Bipolar ICs

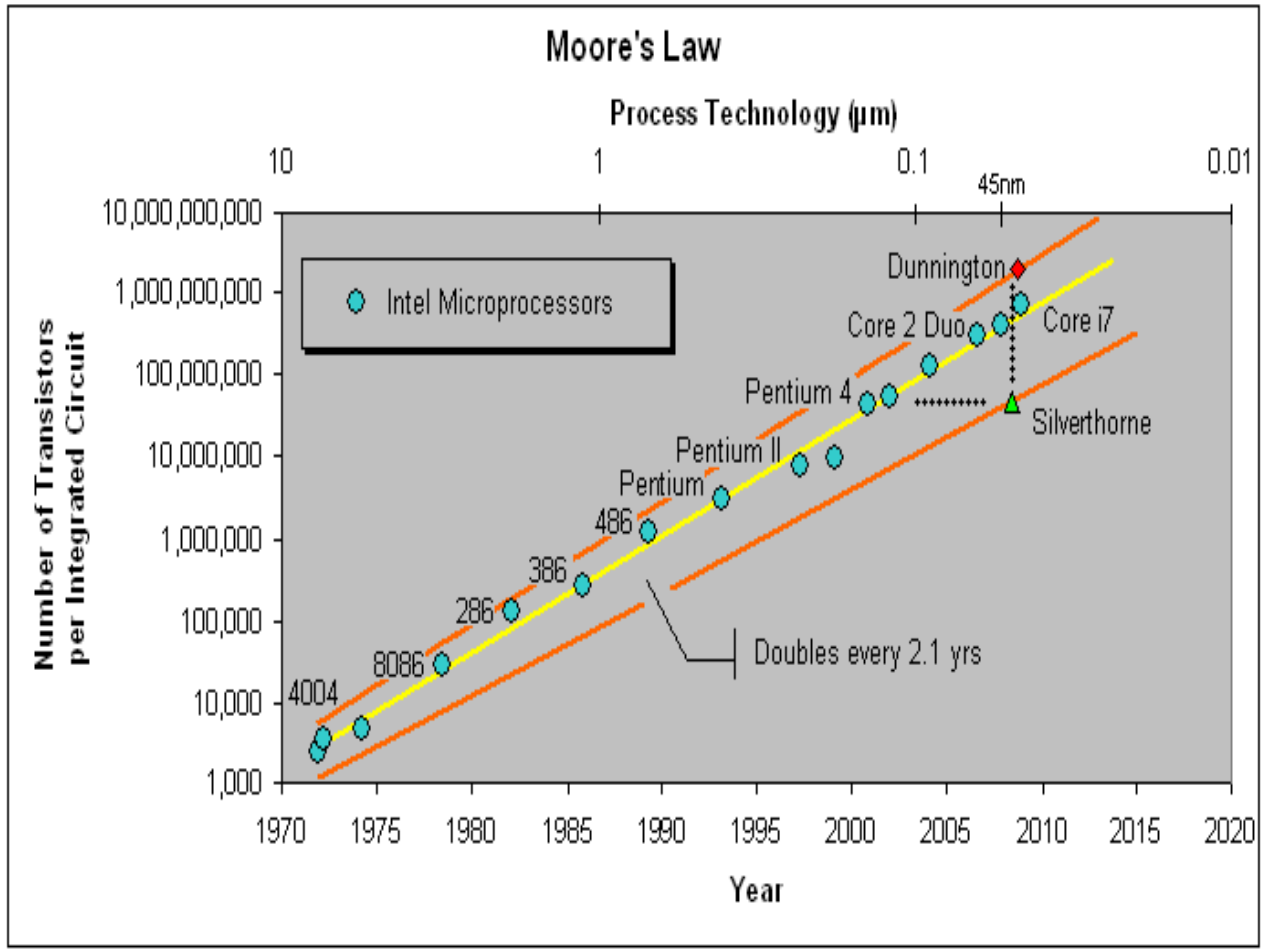


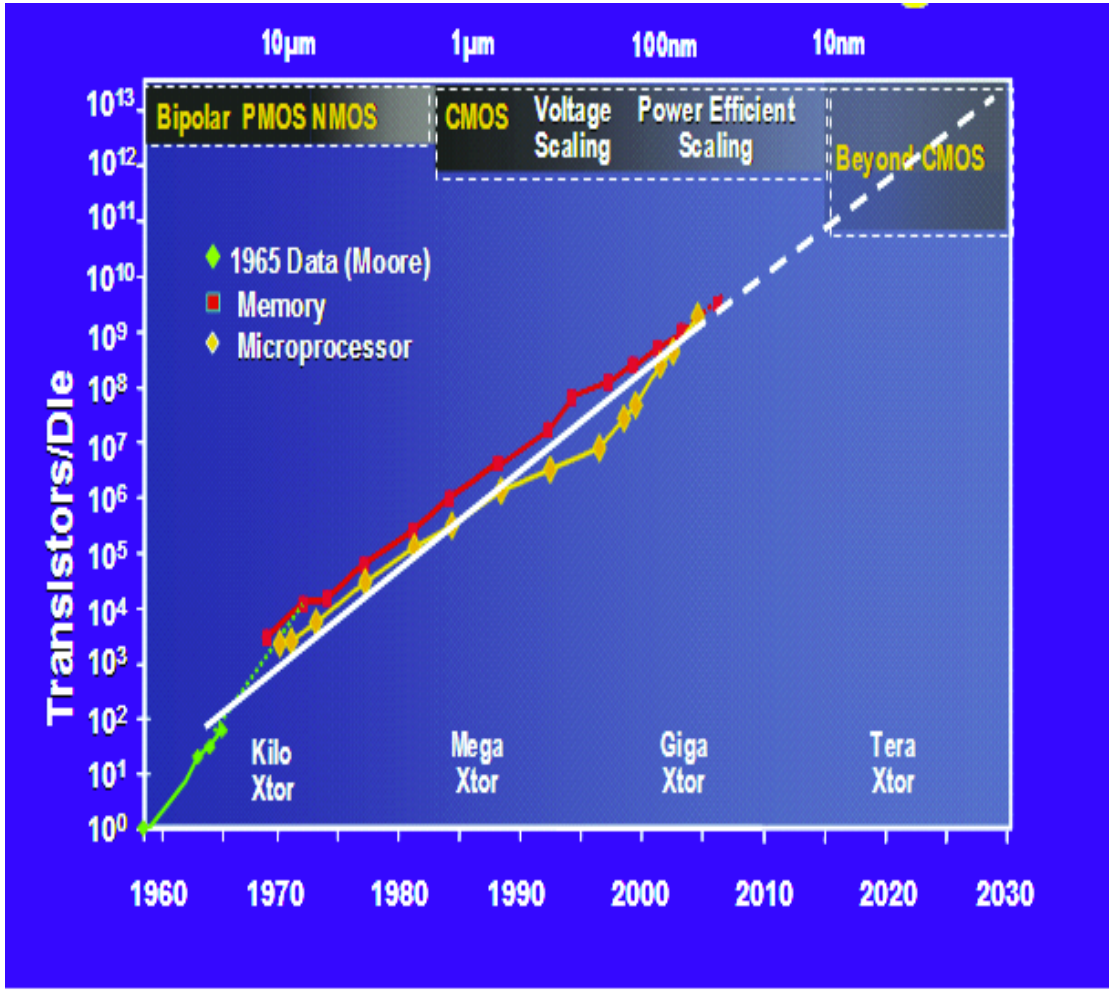


IBM-4341 CPU Board



Moore’s law


Moore's Law
Process Technology (µm)
10
1
0.1
0.01
45nm
Number of Transistors per Integrated Circuit
10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000
Intel Microprocessors
Dunnington
Core 2 Duo
Core i7
Pentium 4
Silverthorne
Pentium II
Pentium
486
386
286
8086
4004
Doubles every 2.1 yrs
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
Year


10µm
1µm
100nm
10nm
Bipolar PMOS NMOS
CMOS
Voltage Scaling
Power Efficient Scaling
Beyond CMOS
1965 Data (Moore)
Memory
Microprocessor
Transistors/Die
Kilo Xtor
Mega Xtor
Giga Xtor
Tera Xtor
1960
1970
1980
1990
2000
2010
2020
2030

Dennard's scaling(1974-MOSFET domination)

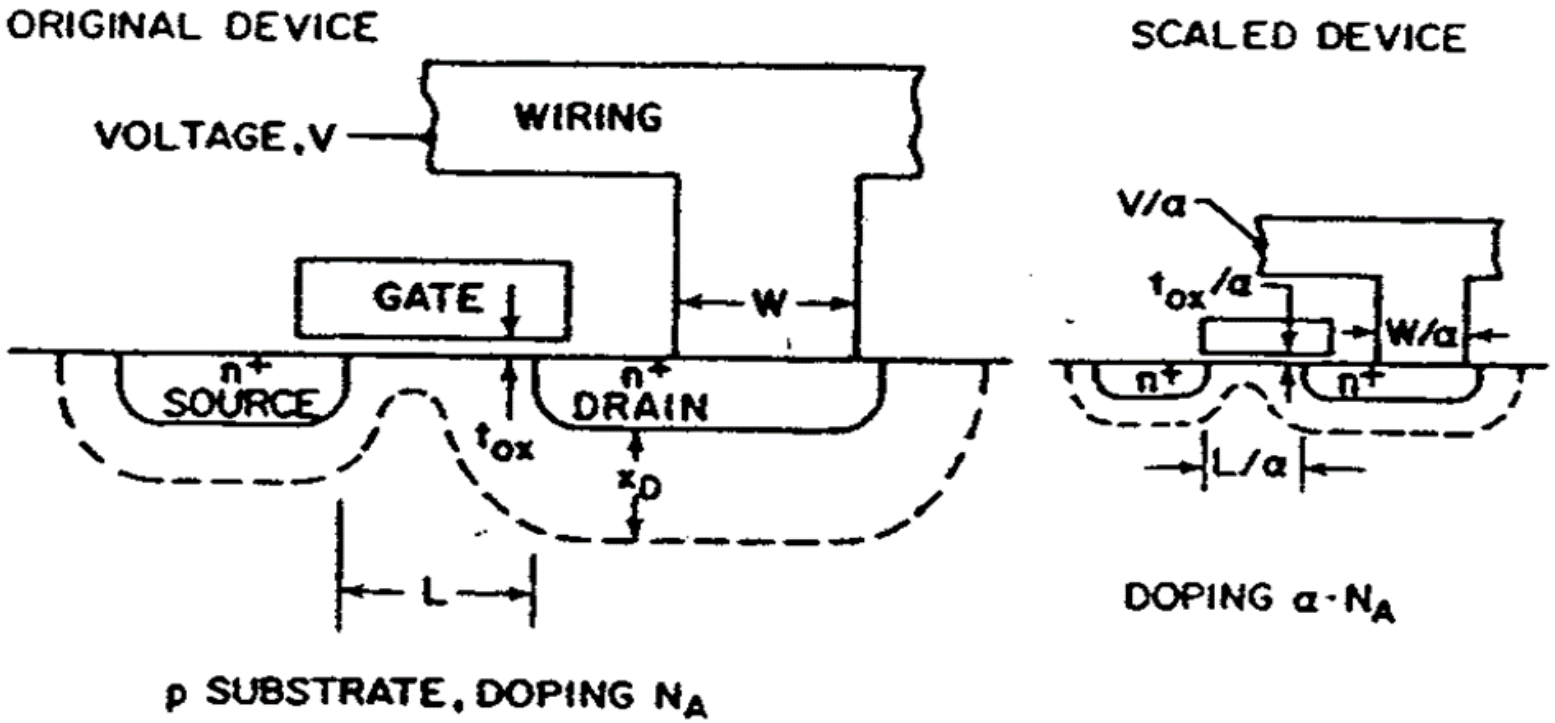
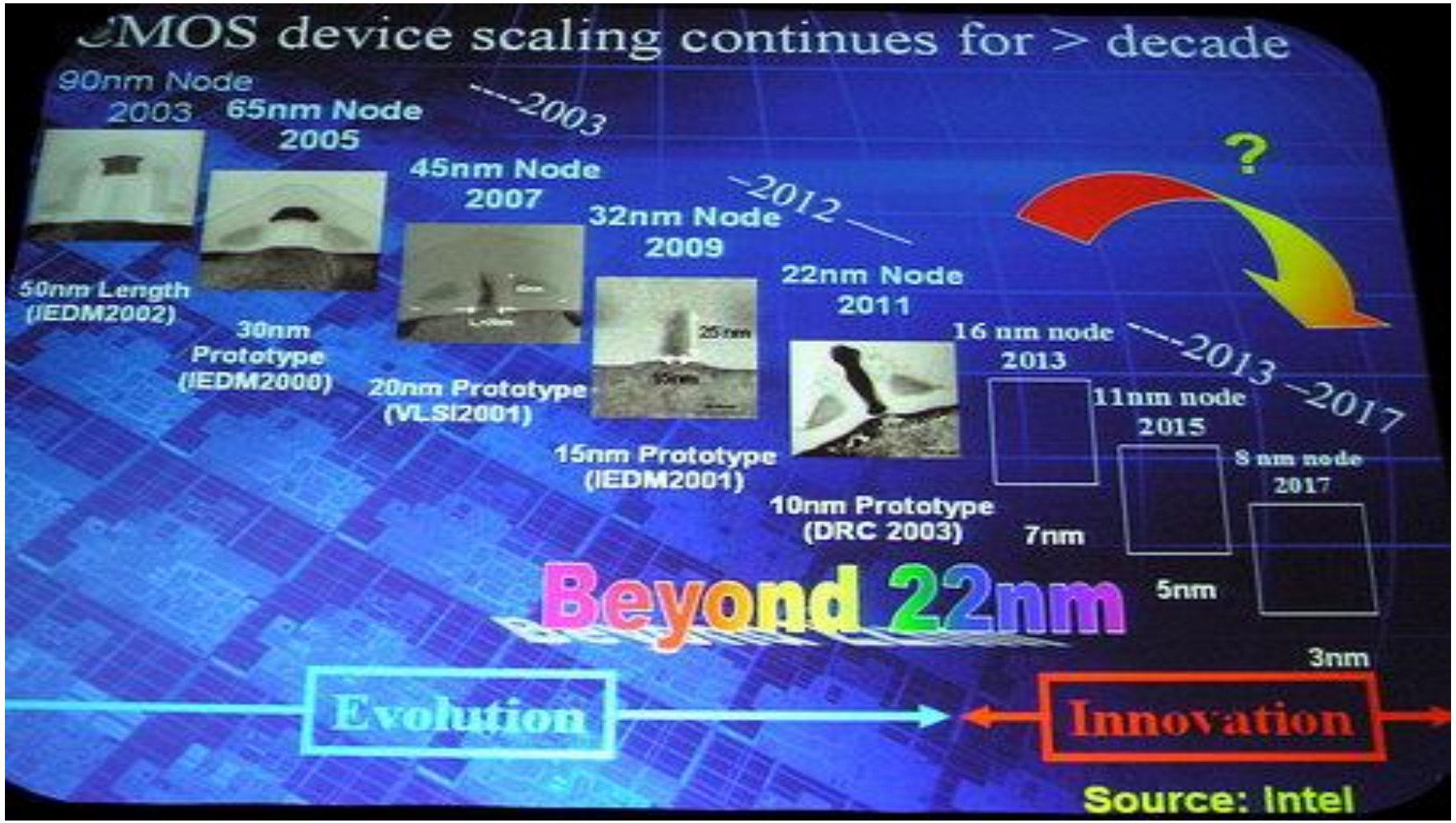


Fig. 1. Principles of constant-electric-field scaling for MOS transistors and integrated circuits.

Technology node



Power consumption with technology nodes

Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm²)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm²)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm²)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5

Problems of plenty??

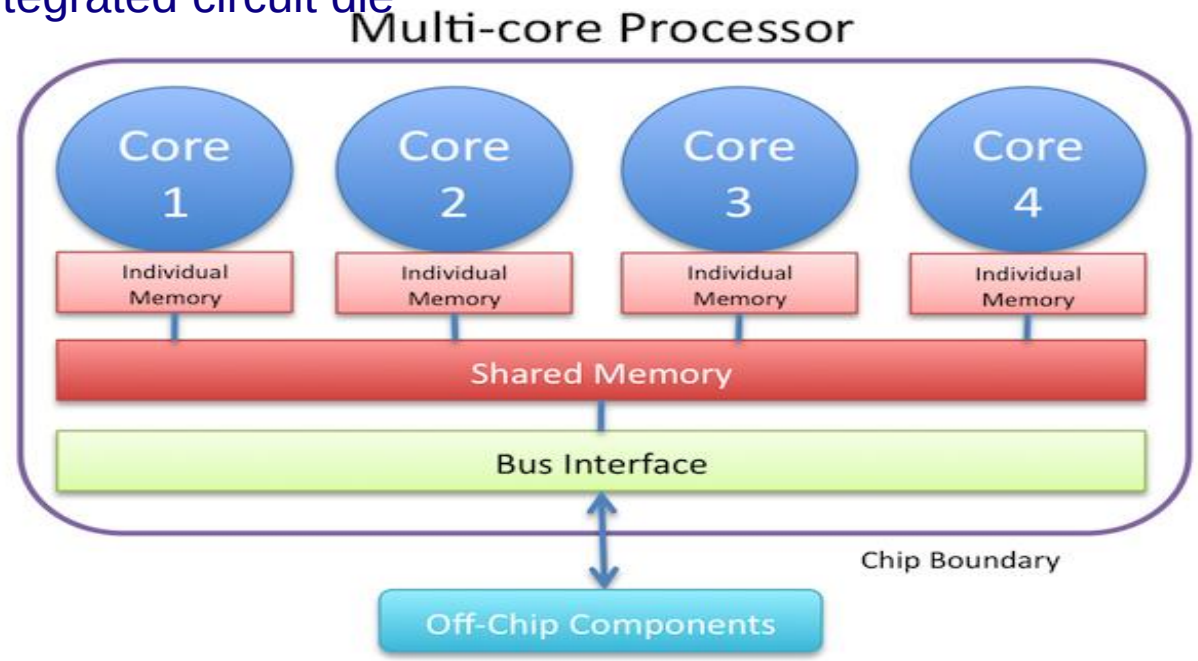
Multi-core processors

Single Core

High Frequency results into:

- Complexity
- High Leakage
- More Heating

A **multi-core processor** is a single computing component with two or more independent processing units called cores, which read and execute program instructions. The instructions are ordinary CPU instructions (such as add, move data, and branch) but the single processor can run multiple instructions on separate cores at the same time, increasing overall speed for programs amenable to parallel computing. Manufacturers typically integrate the cores onto a single integrated circuit die



Where is the catch??

"Effective utilization of the multicore processors is the actual bottleneck. It is the responsibility of the application to take advantage of multiple cores. "

Problems with multicores:

- Lack of parallelism

  Applications doesn't offer the required level of parallelism. Code need to be redesigned to make benefit from multiple cores.

- Off chip bandwidth constraint

  High no of cores puts demand for high off-chip memory. Pin count isn't increasing with no. of cores putting a limit on data access rate.

- Power and Energy constraints

  Power supply can't be reduced indefinitely due to Vt limitations, all cores operating parallelly consumes more power.

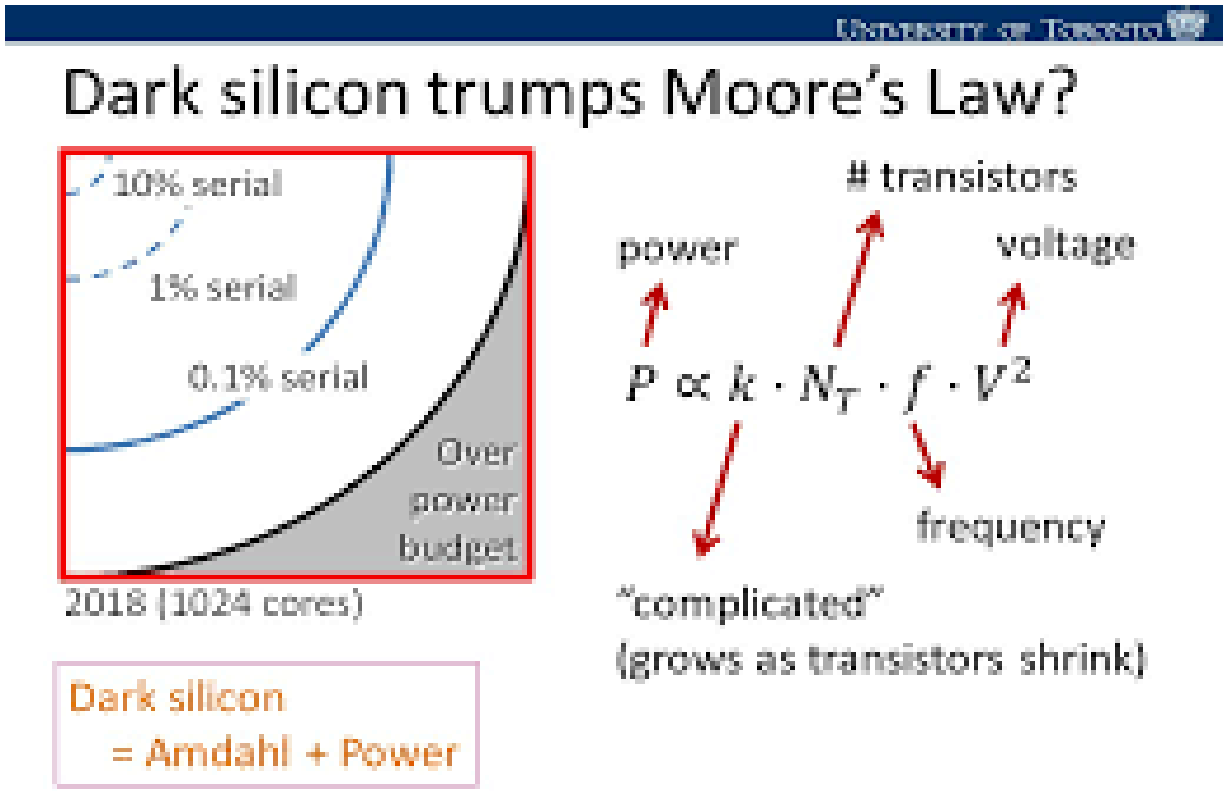
Problem of plenty/multicore

- Amdahl's Law is a law governing the speedup of using parallel processors on a problem, versus using only one serial processor
- Amdahl’s law states that in parallelization, if P is the proportion of a system or program that can be made parallel, and 1-P is the proportion that remains serial, then the maximum speedup that can be achieved using N number of processors is 1/((1-P)+(P/N).

  If N tends to infinity then the maximum speedup tends to 1/(1-P).

  Speedup is limited by the total time needed for the sequential (serial) part of the program.

Dark silicon-problem of plenty!



More transistors coming, but we can't use them

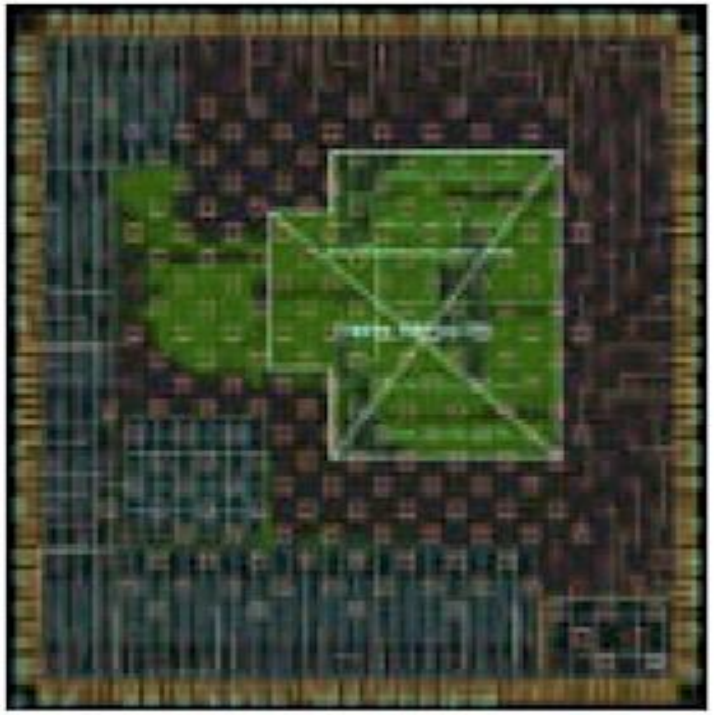
Beware of Dark silicon era!!

With each successive process generation, the percentage of a chip that can actively switch drops exponentially due to power constraints. This means that each time we move to the next process generation, more and more of the chip becomes dark silicon.

What now??

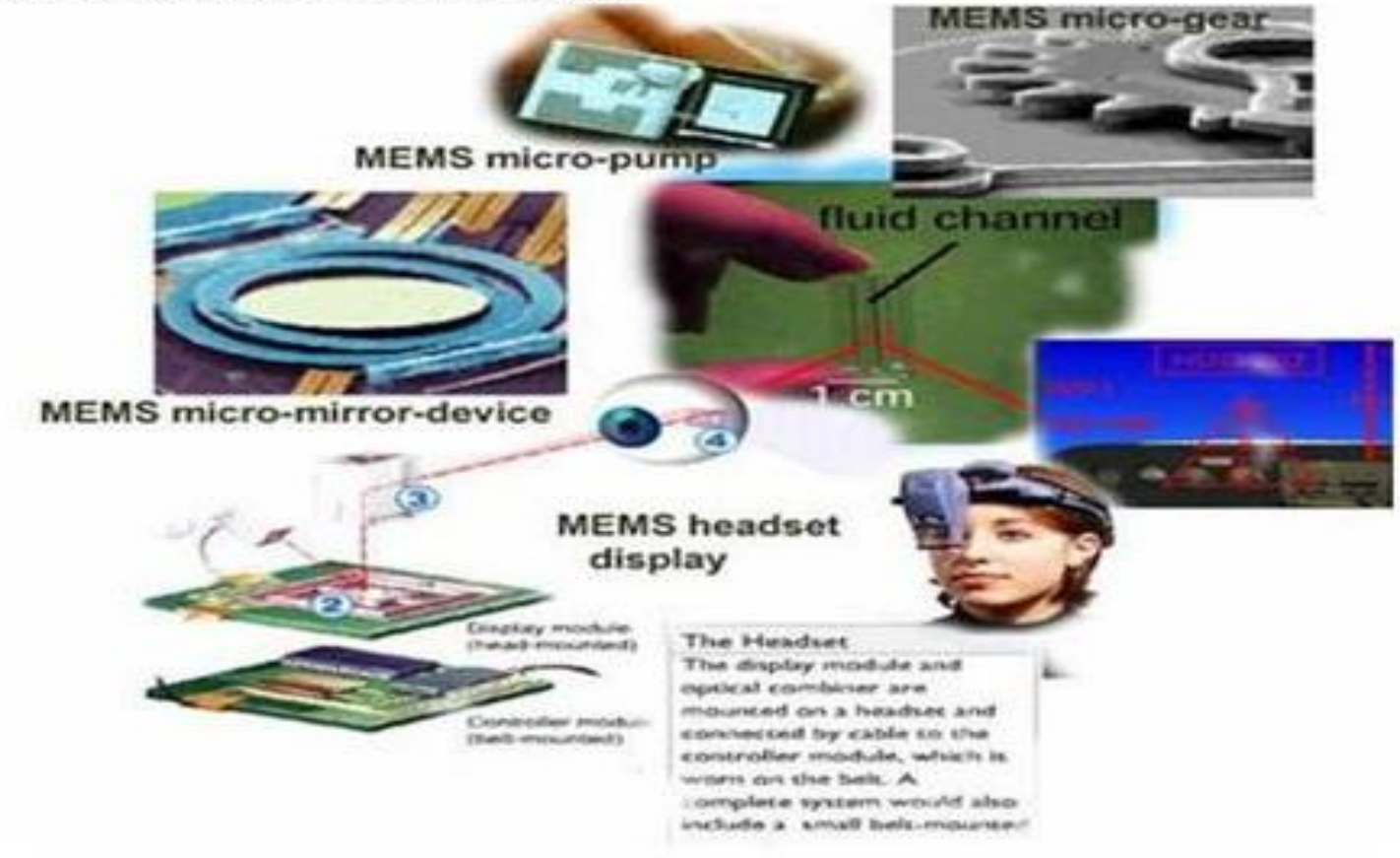
So What Can We Do?

- We **can** have more transistors
- We just can't **power** them all at the same time
- We need to use these extra transistors in new ways
  - Multicores
  - Many-cores
  - Domain-specific processors
- It all points to heterogeneous processing
  - And aggressive power management
- Computing to be done in the most efficient place

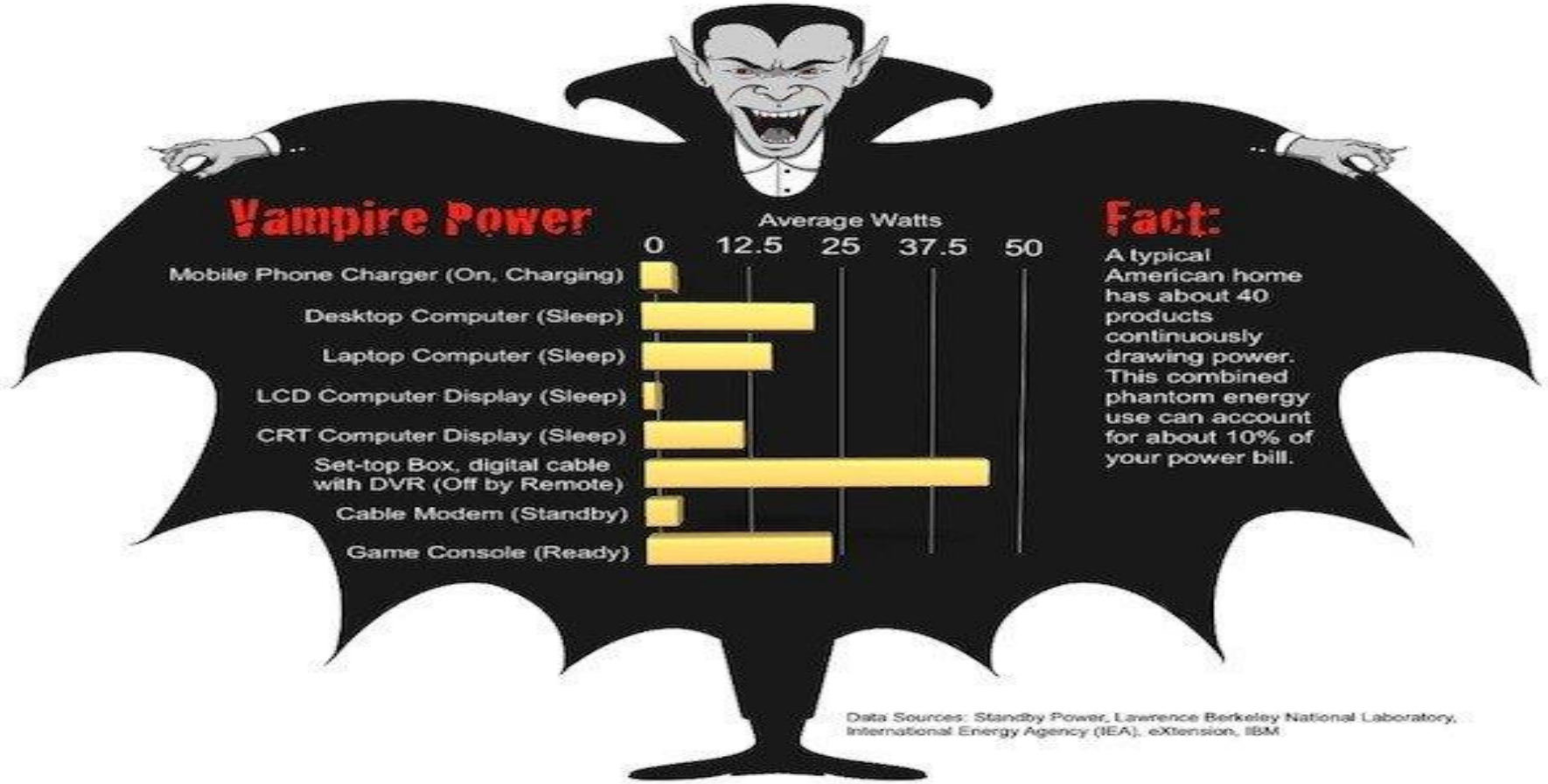


Hetro-integration

Micro-Electro-Mechanical Systems (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology.



Beware of other vampire at home!!



Vampire !! How Much Are They sucking You?

HOW MUCH ARE VAMPIRE ELECTRICAL CHARGES COSTING YOU?

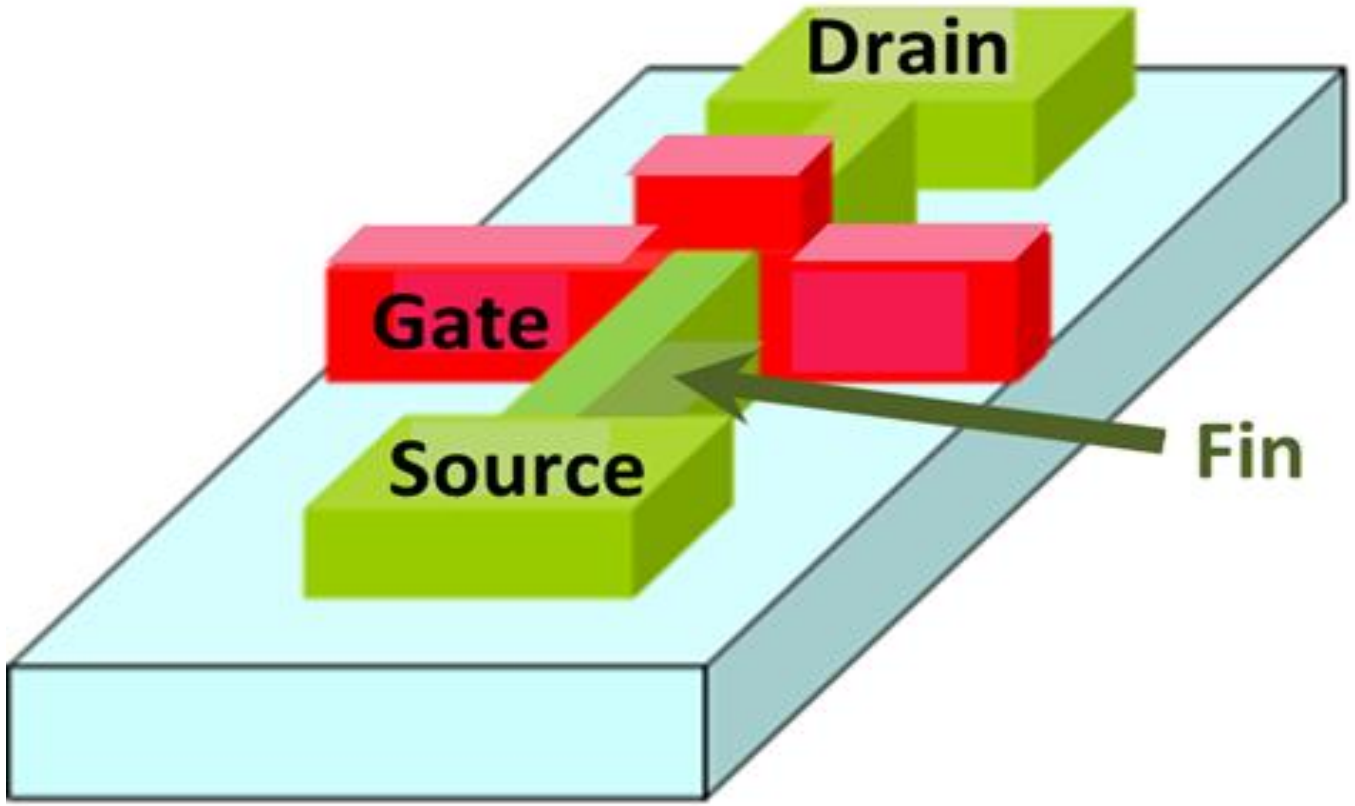
Device/Appliance	Avg. kWh per year	Energy cost per year
Mobile Charger (on, fully charged)	20	$2.00
Computer Display LCD (sleep)	13	$1.30
Desktop Computer including peripherals (on, idle)	250	$25.00
Laptop Computer (on, fully charged)	40	$4.00
Laser Printer (off)	14	$1.40
DVR (on, no recording)	140	$14.00
Digital Cable Box (on, TV off)	230	$23.00

Device/Appliance	Avg. kWh per year	Energy cost per year
VCR (on, not playing)	70	$7.00
CD Player (On, not playing)	37	$3.70
Audio Mini System (CD, not playing)	130	$13.00
Coffee Maker (off)	10	$1.00
DVD Player (On, Not Playing)	68	$6.80
Game Console (ready)	210	$21.00
Microwave Oven (ready)	30	$3.00

Device architectures evolution in the recent past

- Strained silicon
- SOS, SOI
- High K –Metal gate MOSFET
- FinFET (Trigate MOSFET)

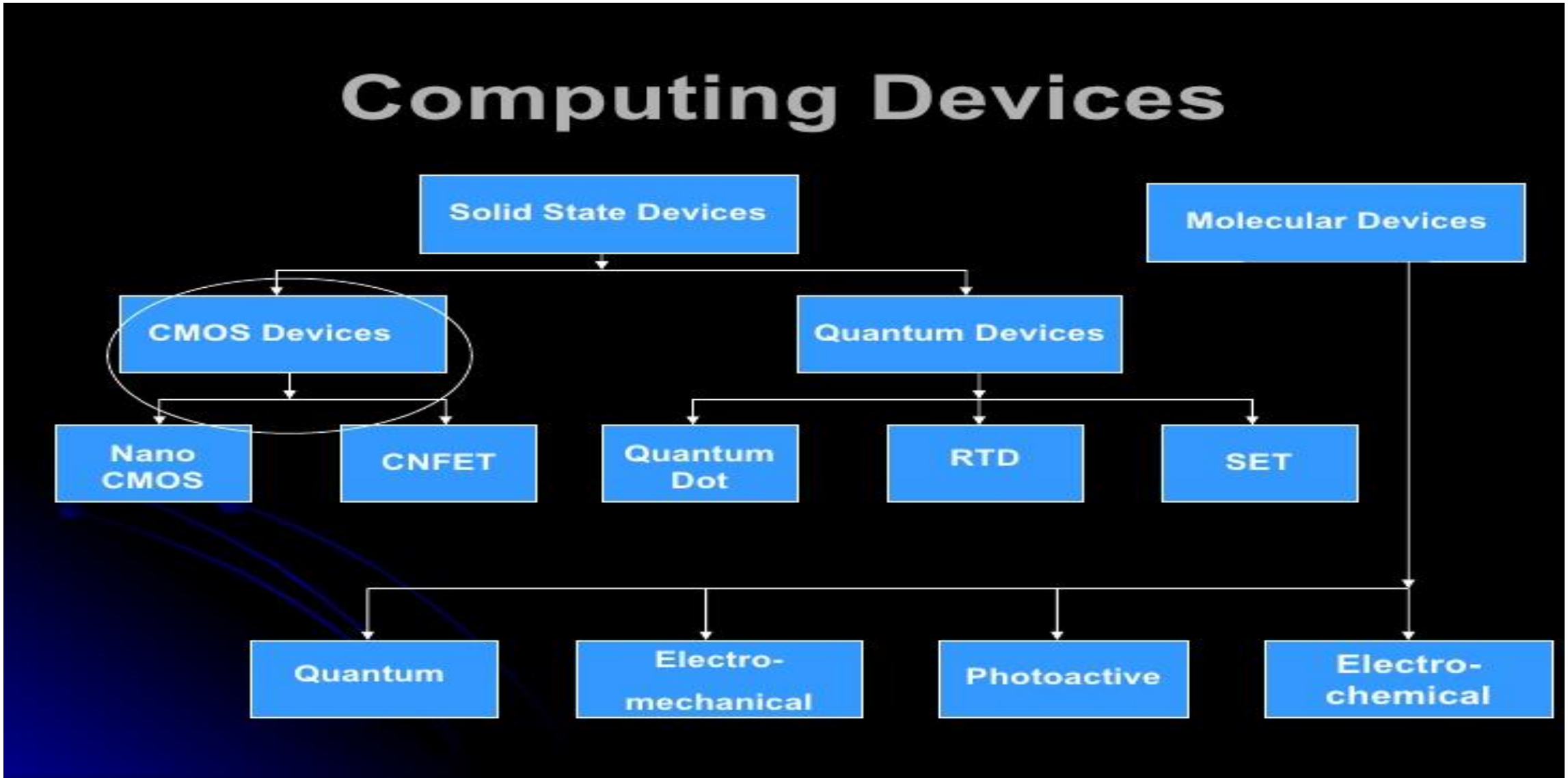
Latest device architecture(commercial applications since 2011)



Do not focus on numbers but performance

- High performance.(Quality matters not quantity)
- Use only a single device if possible to all circuits-in our case MOSFET or any other device Put more devices to speed up-parallel processing.
- Use batch processing to keep cost down.
- Now emphasis is on performance not on Moore’s law
- **Or the more the merrier is no more attractive!!**
- **Alternate architecture for computation-Quality matters not quantity!!**

What to look forward



Device astrology

- What is it?
- Why is it important?
- Can we do it?
- How to go about it?

What is it?

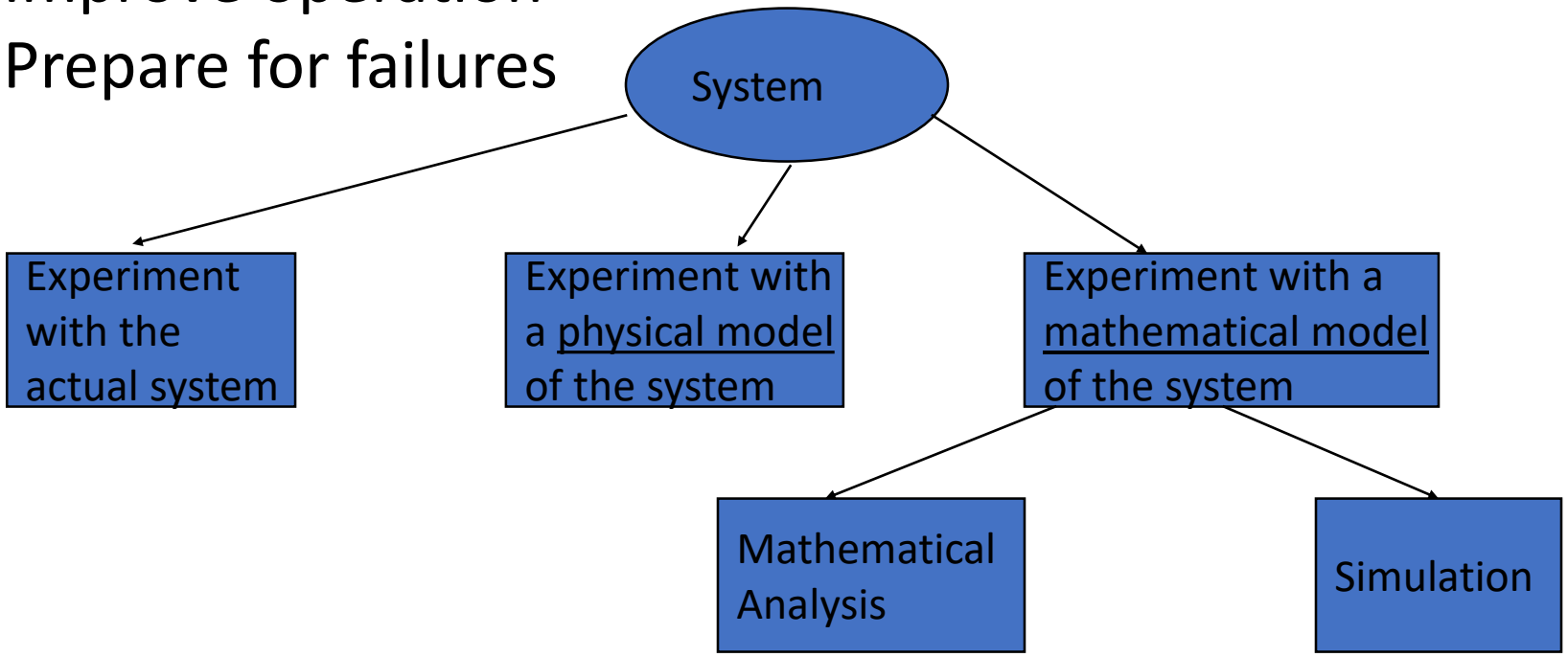
- It is about prediction of future/
- Giving details before it is born
- Help us in planning
- Unfortunately in our life it is not possible
- But good part in the case of devices it is possible at least to a great accuracy and reliable

What is simulation?

“Simulation is the process of designing a model of a real system and conducting experiments with this model for the purpose of either understanding the behavior of the system and/or evaluating various strategies for the operation of the system.”

WHY & HOW TO STUDY A SYSTEM

Measure/estimate performance
Improve operation
Prepare for failures



Allows us to:

- Model complex systems in a detailed way
- Describe the behavior of systems
- Construct theories or hypotheses that account for the observed behavior
- Use the model to predict future behavior, that is, the effects that will be produced by changes in the system
- Analyze proposed systems

THE NATURE OF SIMULATION

- *Simulation*: Imitate the operations of a system or process, usually via computer
  - To study system, often make assumptions/approximations, both logical and mathematical, about how it works
  - These assumptions form a *model* of the system
  - If model structure is simple enough, could use mathematical methods to get exact information on questions of interest — *analytical solution*

The Nature of Simulation (cont'd.)

- But most complex systems require models that are also complex (to be valid)
  - Must be studied via simulation — evaluate model numerically and collect data to estimate model characteristics

The Nature of Simulation (cont'd.)

- Impediments to acceptance, use of simulation
  - Models of large systems are usually very complex
    - But now have better modeling software … more general, flexible, but still (relatively) easy to use
  - Can consume a lot of computer time
    - But now have faster, bigger, cheaper hardware to allow for much better studies than just a few years ago … this trend will continue
    - However, simulation will also continue to push the envelope on computing power in that we ask more and more of our simulation models
  - Impression that simulation is "just programming"
    - There's a lot more to a simulation study than just "coding" a model in some software and running it to get "the answer"
    - Need careful design and analysis of simulation models – simulation methodology

HOW TO SIMULATE

- By hand
- Spreadsheets
- Programming in General Purpose Languages
- Simulation Languages
- Simulation Packages

Issue: Modeling Flexibility vs. Ease of Use

What is the role of CAD/simulation in MICROELECTRONICS?

Name CAD brings to our mind ECAD or EDA(ELECTRONICS DESIGN AUTO MATION) mainly tools developed for the design process

Chip making-designing & fabricating –complex task- so the approach is DIVIDE& CONQUER??

Design side –Heard of top down, bottom up and mixed methodology etc???

Another CAD ??

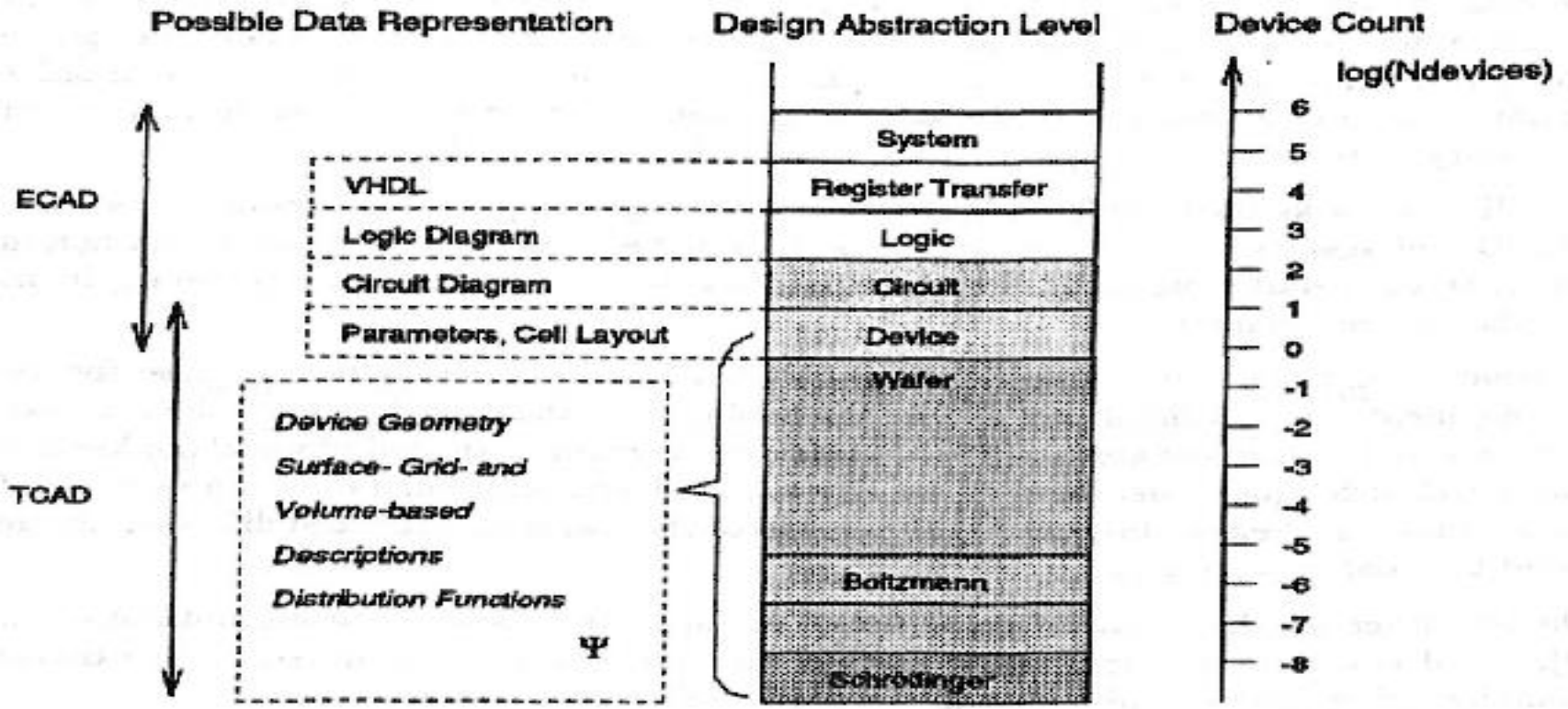
TCAD-often paid less attention-love to hate

- What is it? It is Process and device simulation. used for the design of new VLSI devices and

Processes.

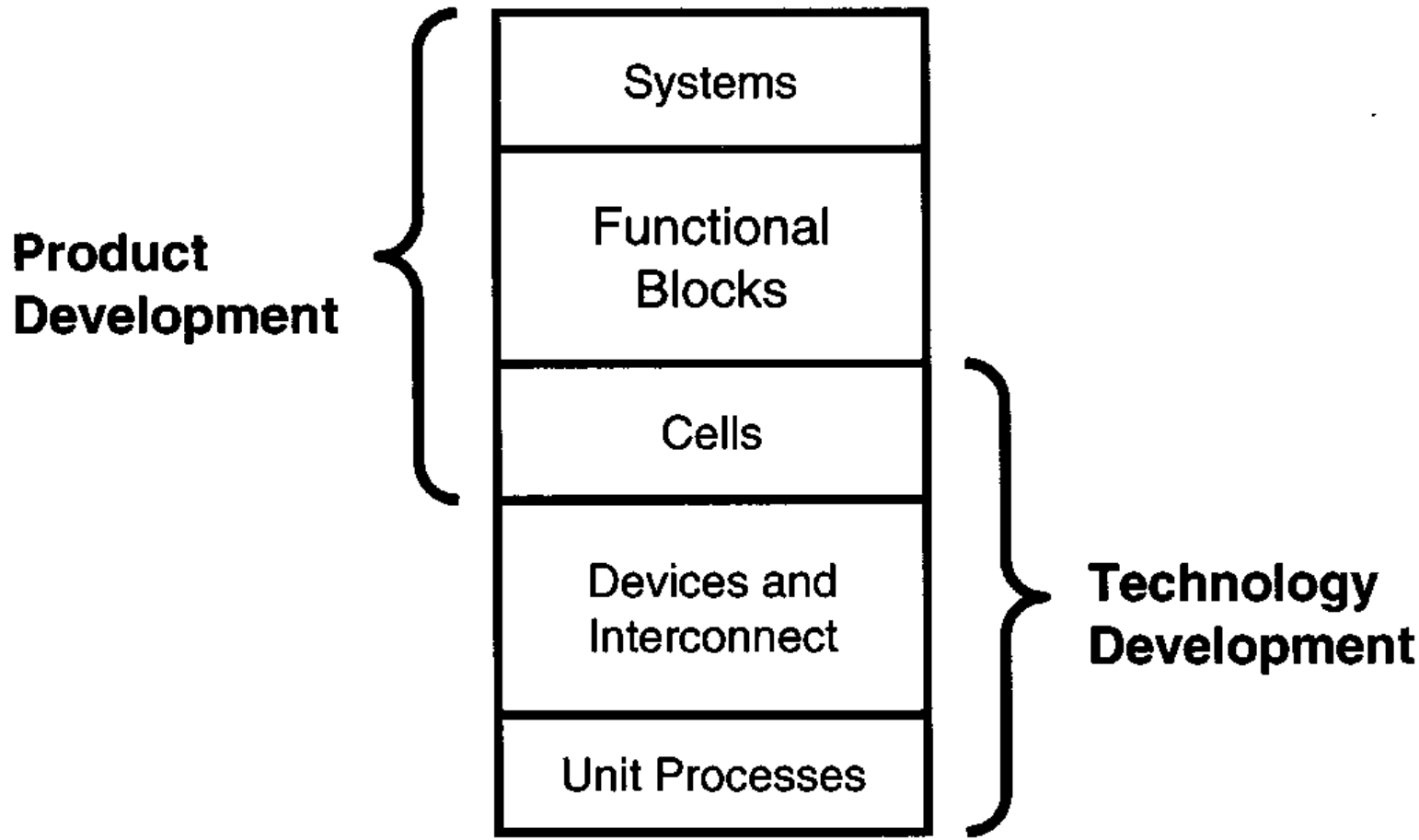
an explorative tool to gain a better understanding of process and *device physics*

ECAD & TCAD

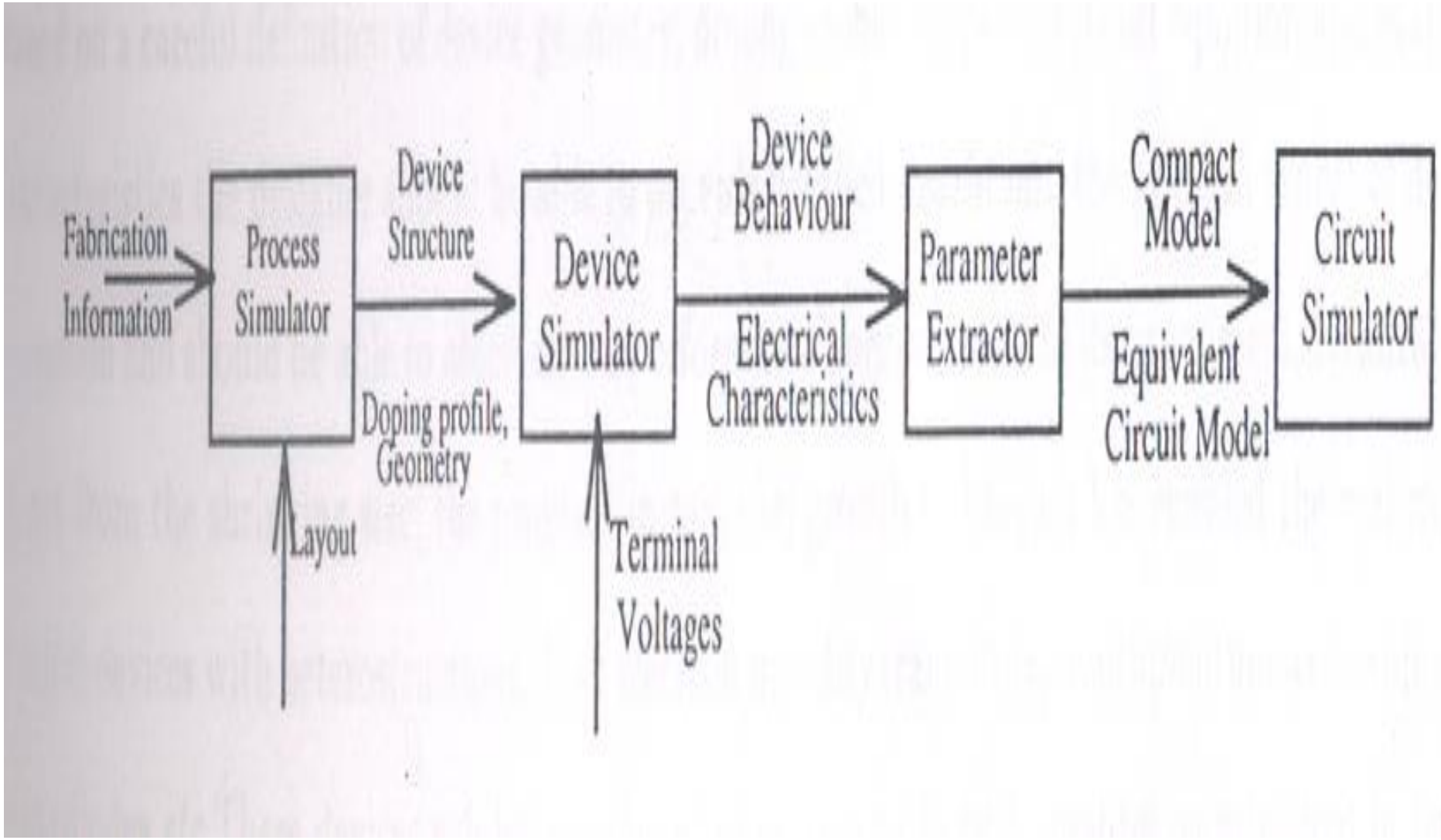


Design levels and device count scale in ECAD and TCAD

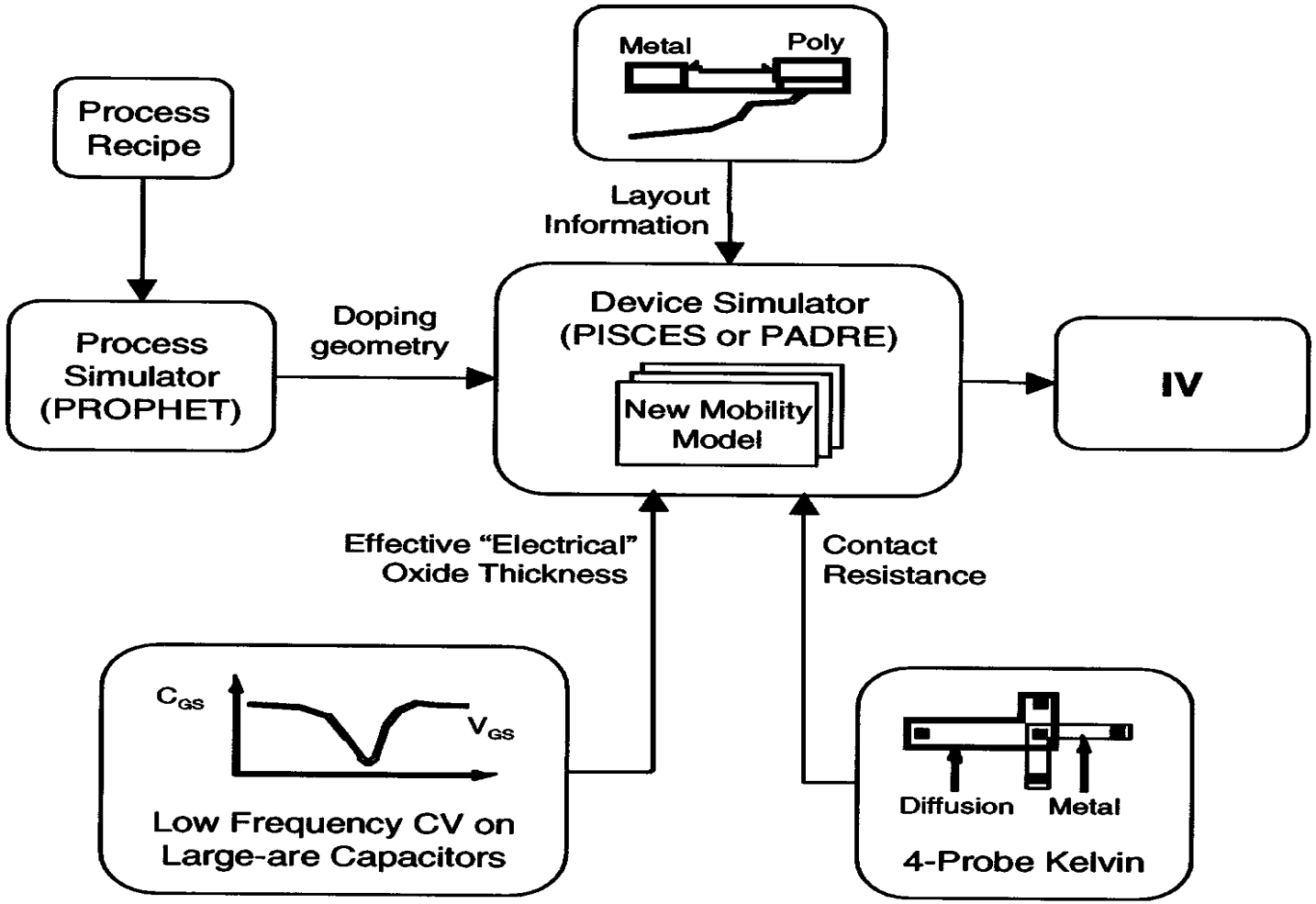
Layers of IC development



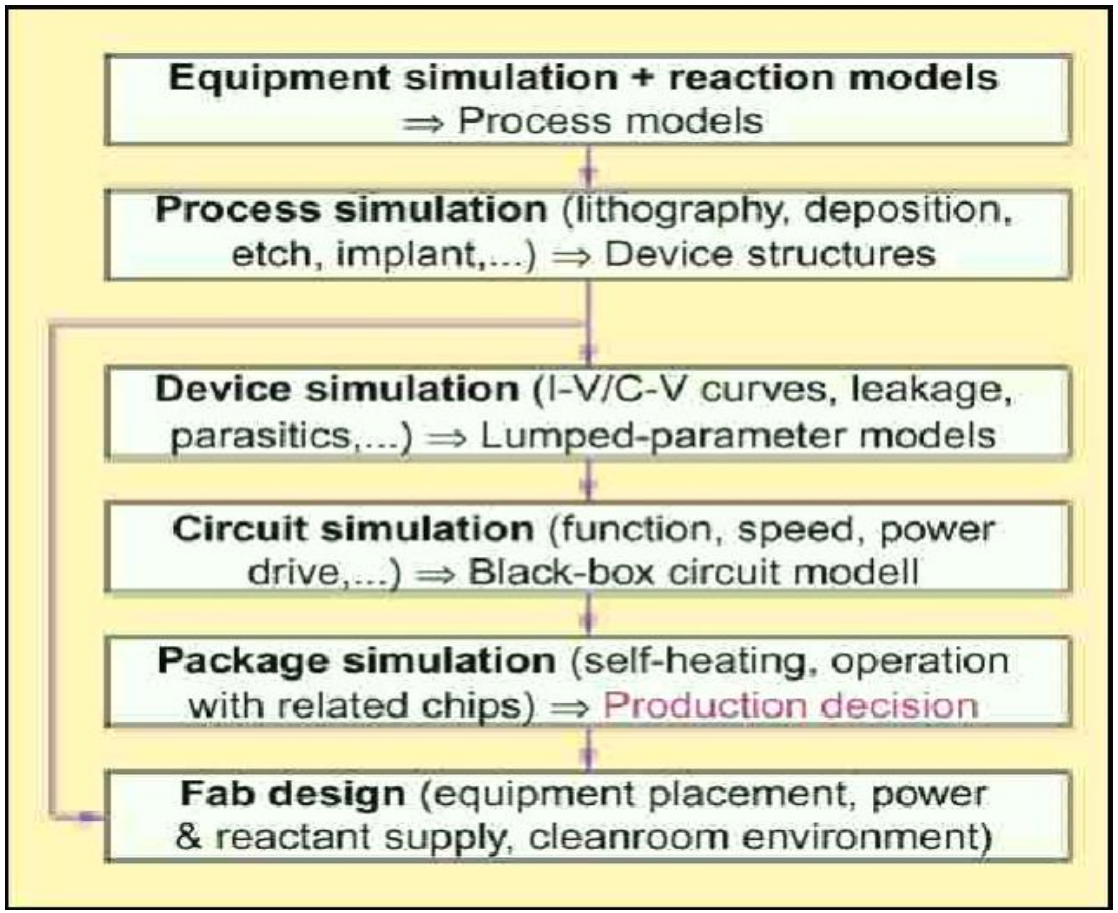
Inter relationship between process,Device and circuit simulator



TCAD-based IV characterization



THINGS involved in TCAD



VIRTUAL FAB

We must run an accurate process simulation to get device structure that produces a meaningful device simulation…In fact, the ultimate platform for TCAD would be a *Virtual Fab*.

In a virtual fab, all aspects of electronics production can be simulated and debugged before production starts, or even before the fabrication plant comes on-line

Benefits of Device Simulation

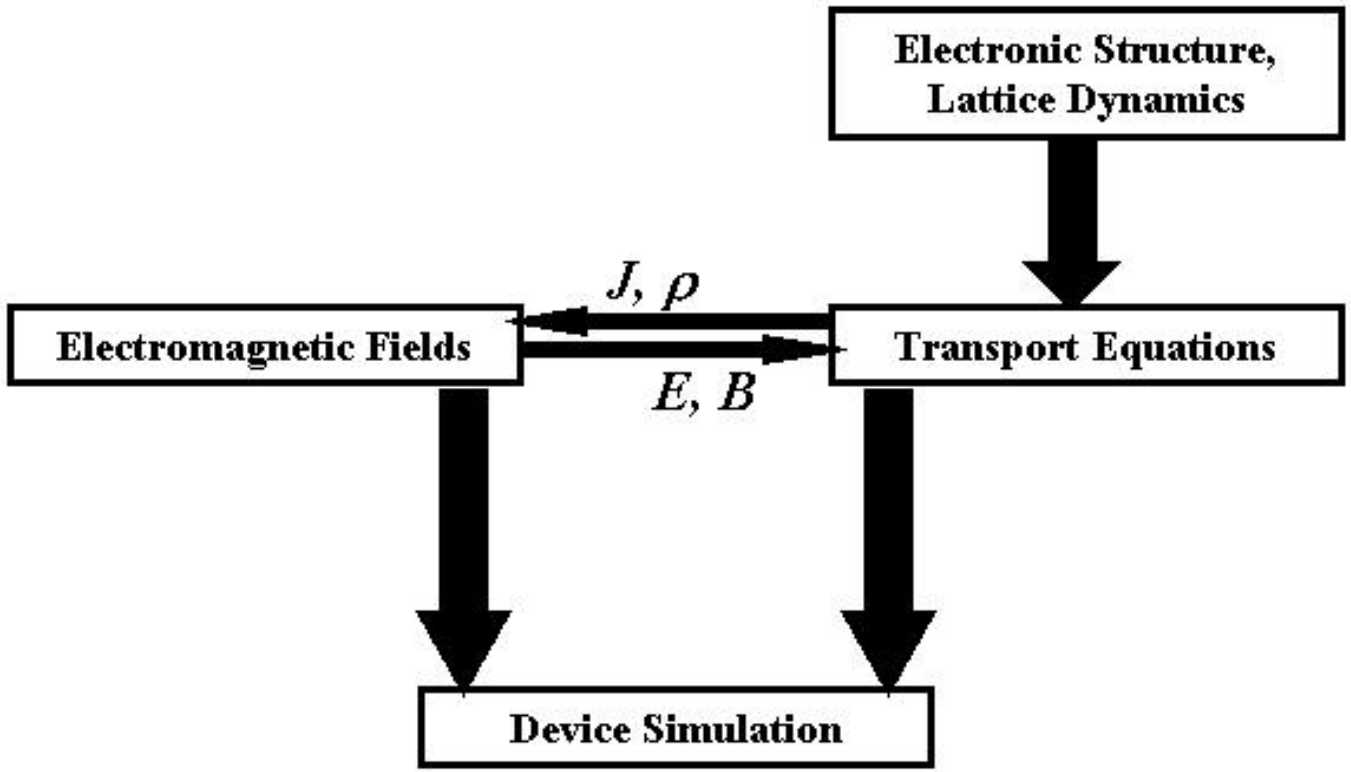
- Allows you to probe inside device where measurements can not be made.
- Explore new experimental devices and device phenomena without fabricating device.
- Educate researchers, engineers and students to expand the frontiers of mathematical and computational skills germane to microelectronics.
- Help develop CAD tools so industry can continue its march forward in the miniaturization of electronic devices and circuits.

Device modeling

- Development of models-1.Mathematical vs equivalent circuit models
- Mathematical models—Physical and empirical

(Physical models are based on carrier transport equations ie. Physics based) Device models output is expected to give I-V characteristics of the device which could be utilized in Circuit simulation

A schematic description of the device simulation sequence



Classification (Based on PHYSICS)

- Classical or more aptly semiclassical appraches

DRIFT DIFFUSION EQUATIONS

HYDRODYNAMIC EQUATIONS

Particle based-MONTE CARLO techniques

Classification (Based on PHYSICS) Continued

- Introduction of of quantum corrections

Inclusion of Tunneling and Size-Quantization Effects in Semi-Classical Simulators

Tunneling Effect: WKB Approximation and Transfer Matrix Approach

Quantum-Mechanical Size Quantization Effect

Drift-Diffusion and Hydrodynamics: Quantum Correction and Quantum Moment Methods

Particle-Based Device Simulations: Effective Potential Approach

Classification (Based on PHYSICS) Continued

- Full Quantum

Quantum Transport

Direct Solution of the Schrodinger Equation (

Atomistic Simulations – The Future

Two legs of device simulator(At least in classical case)

- Poisson's equation and Boltzmann Transport Equation(BTE).

(Once you can formulate Poisson's equation and solve it you have the electric field and potential information available and one can deduce I-V characteristics from it)

BTE upto the device size where quantum effects become significant, semi-classical model based on BTE could be used to describe carrier transport

BTE

- BTE is based on on the dynamical laws followed by a carrier located in the energy bands of the material.
- It describes the time evolution of the carrier distribution f(r,k,t) in a six dimensional phase space under the influence various internal and external forces
- BTE is semi-classical

Validity of BTE

- The scattering probability is independent of external forces.
- Collision duration is much smaller than free flight duration
- The band theory and the effective mass theorem apply to semiconductor under consideration.

Semiclassical Models

All contain Poisson Equation + Transport Equation

Boltzmann Transport Equation Model:

$$\nabla^2\phi = \frac{q}{\varepsilon_s}\left[\int f\left(\vec{r},\vec{k},t\right)d\vec{k} - p\left(\vec{r},t\right) + N_A\left(\vec{r}\right) - N_D\left(\vec{r}\right)\right]$$

$$\frac{\partial f}{\partial t} + \frac{1}{\hbar}\nabla_{\vec{k}}\varepsilon\left(\vec{k}\right)\cdot\nabla_{\vec{r}}f + \frac{q}{\hbar}\nabla_{\vec{r}}V\left(\vec{r},t\right)\cdot\nabla_{\vec{k}}f = \left(\frac{\partial f}{\partial t}\right)_{coll}$$

$$\vec{r}\in\mathbf{R}^3, \vec{k} = \left(k_x,k_y,k_z\right)$$

Hydrodynamic Model:

$$\nabla^2\phi = -\frac{q}{\varepsilon}\left(-n + p + N_D^+ - N_A^-\right)$$

$$q\frac{\partial n}{\partial t} = \nabla\cdot\vec{J}_n - q\left(R - G\right)$$

$$\frac{\partial\vec{v}}{\partial t} + \left(\nabla\cdot\vec{v}\right)\vec{v} + \frac{k_B}{m^*n}\nabla\left(nT\right) - \frac{q}{m^*}\nabla V = C_{\vec{u}}$$

Drift-Diffusion Model:

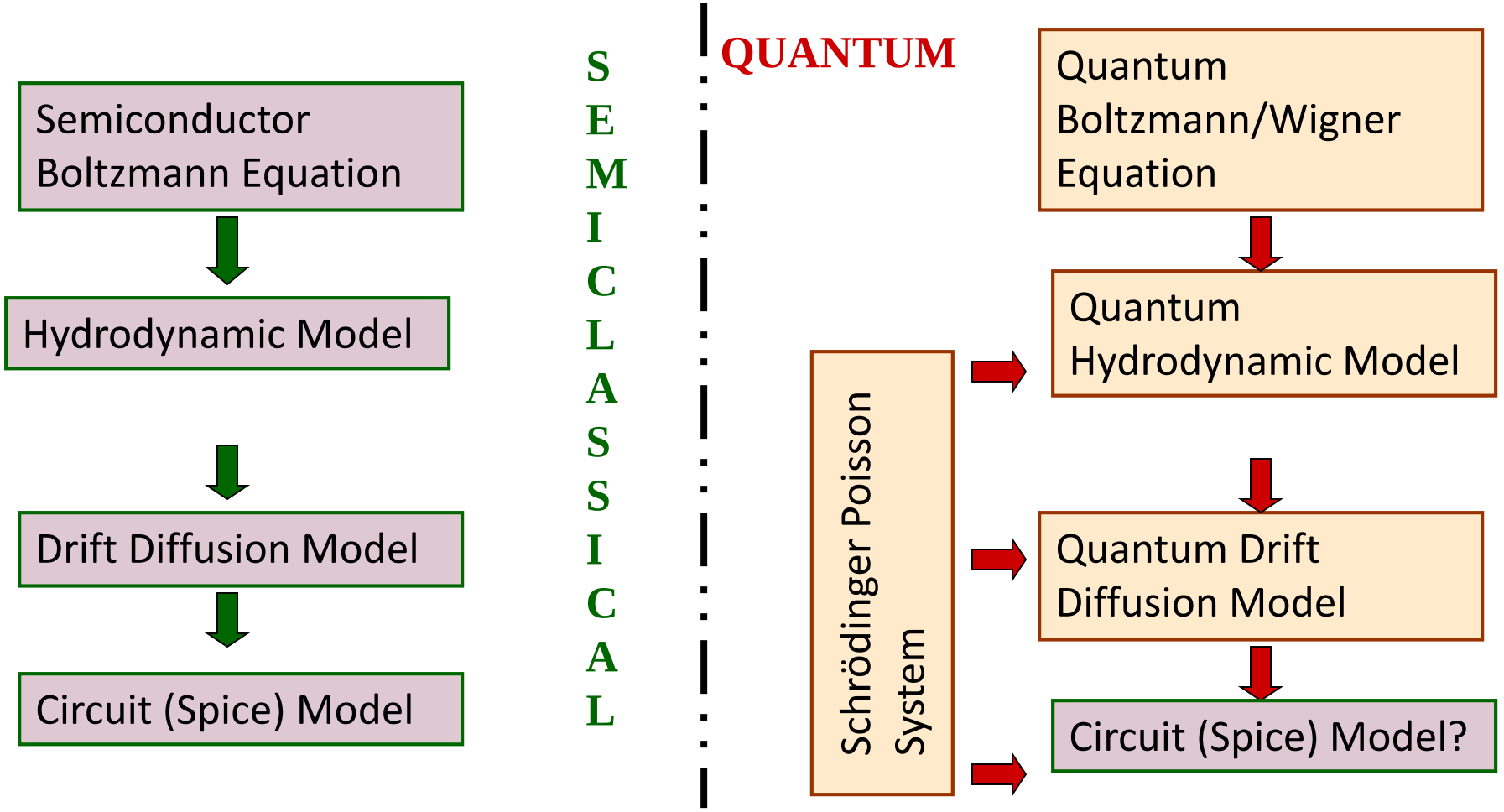
$$\nabla^2\phi = -\frac{q}{\varepsilon}\left(-n + p + N_D^+ - N_A^-\right)$$

$$q\frac{\partial n}{\partial t} = \nabla\cdot\vec{J}_n - q\left(R - G\right)$$

$$\vec{J}_n = -qn\mu_n\nabla\phi + qD_n\nabla n$$

Transport equations are shown here only for electrons. Transport equations for holes are analogous and understood.

Semiconductor Simulation Models: Hierarchy



Challenges for device modeling

- MOS device vs non-conventional MOS.

Demand of scaling and ITRS

Device performance may be improved by (1) inducing a larger charge density for a given gate voltage drive; (2) enhancing the carrier transport by improving the mobility, saturation velocity, or ballistic transport; (3) ensuring device scalability to achieve a shorter channel length; and (4) reducing parasitic capacitance and parasitic resistance.

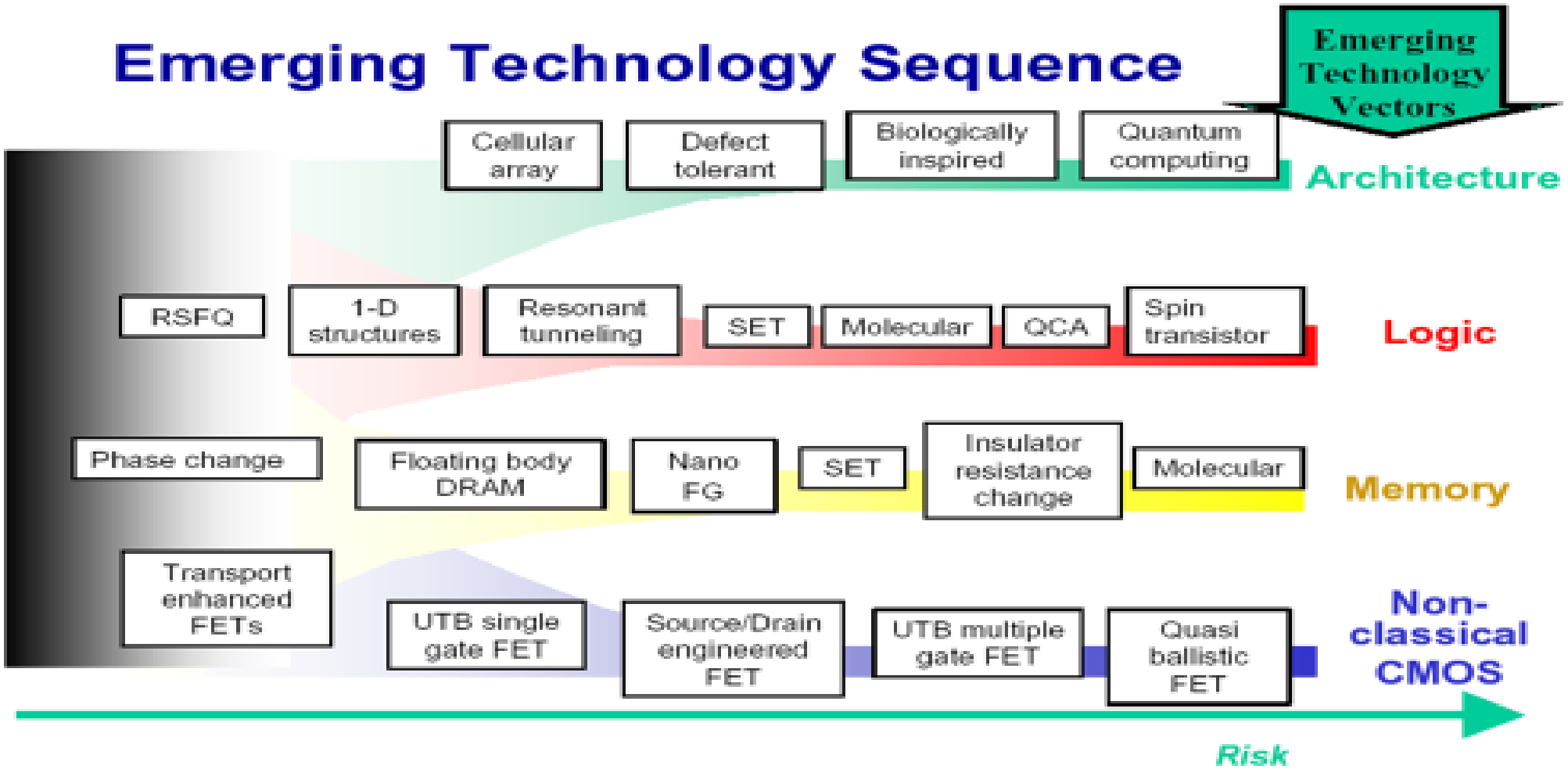
Device performance improvement opportunities

Source of improvement	Parameters affected	Method
Charge density	1. S (inverse subthreshold slope) 2. Q_{inv} at a fixed off-current	1. Double-gate FET 2. Lower the operating temperature
Carrier transport	1. Mobility μ_{eff} 2. Carrier velocity 3. Ballistic transport	1. Strained silicon 2. High mobility and saturation velocity materials (e.g. Ge, InGaAs, InP) 3. Reduce mobility degradation factors (e.g. reduce transverse electric field, reduce Coulomb scattering due to dopants, reduce phonon scattering) 4. A shorter channel length 5. Lower the operating temperature
Ensure device scalabilty to a shorter channel length	1. Generalized scale length (λ) 2. Channel length (L_g)	1. Maintain good electrostatic control of channel potential (e.g. double-gate FET, ground-plane FET, and ultra-thin body SOI) by controlling the device physical geometry and providing means to terminate drain electric fields 2. Sharp doping profiles, halo/pocket implants 3. High gate capacitance (thin gate dielectrics, metal gate electrode) to provide strong gate control of channel potential
Parasitic resistance	1. R_{ext}	1. Extended/Raised source/drain 2. Low-barrier Schottky contact
Parasitic capacitance	1. C_{jn} 2. C_{GD}, C_{GS}, C_{GB}	1. SOI 2. Double-gate FET

Looking ahead

- What is emerging

How things fit



Careers for New EE Graduates…

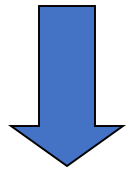
- Technology Development
  - –Process/Device Architecture
  - –Fabrication
    - Unit Process Development
    - Process Integration
  - –TCAD
  - –Compact Modeling
  - –Electronic Test
  - –Reliability

- FablessTechnology Support
  - –Increasing demand as fabrication moves off-shore

- Research

common denominator is team work:

Device Physics, Engineering Statistics



Need for strong background in above disciplines

Device Physics Education

First Level

–Better balance between MOSFETs (current emphasis) and other essential devices

–BJTs: they are still present in VLSI designed-in or parasitic devices!

–First-order analytical models preferred, where available

–Even crude, qualitative models are useful as “mental crutches” in analysis of new situations

Second Level

–In-depth treatment of MOSFETs and BJTs

–Well proven new physical models -to be discovered in recent literature and included in textbooks

–De-emphasize teaching on volatile knowledge such as on latest ITRS “technology boosters”, etc., except for optional reading

–Good references for individual study, including HBTs, promising nanoelectronic devices, etc.

Ultimate Goal, Device Physics Education

"Capability to stand up to and reject or modify the results of a computer-aided design"

ALL simulations are to inform not to impress!!!

Current major suppliers of TCAD tools
Synopsys- *www.synopsys.com*
Silvaco -*www.silvaco.com*
Crosslight- *www.crosslight.com*
Cogenda Software|VisualTCAD--
www.cogenda.com

Open source :1. Archemedes -
www.gnu.org/software/archimedes/
2. NanoHub - *www.nanohub.org*

Thank you but do not forget to your put Hands on link given
(Rewards a simple device simulator which can be installed on your window PC with its manual and references used in this lecture preparation or any query
Contact me at bprasad2005@gmail.com)

Link:
http://thequestforum.org/quiz/handsonymca/index.html